22/07/24

Unit ⇨ 4

Monday

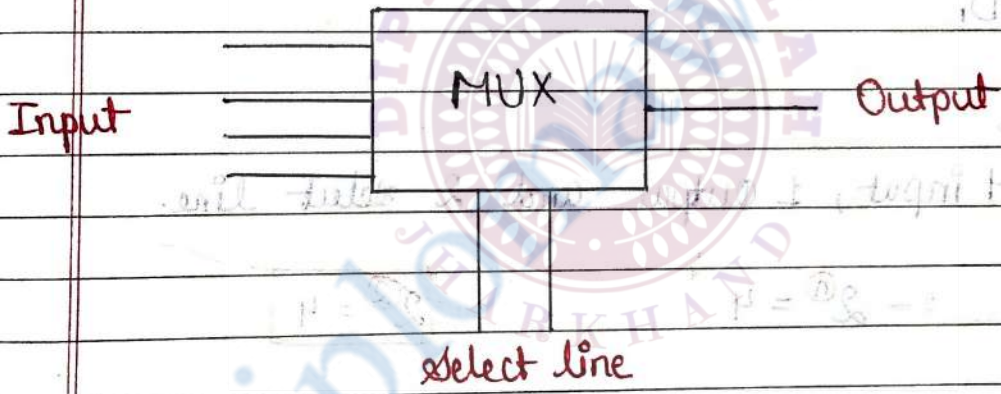
PAGE

DATE / /

Multiplexers and Demultiplexers

Multiplexer (Mux) : Data selector

(Many to one)



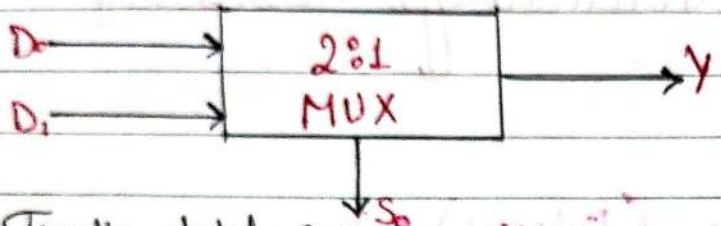
Input		Output
2	:	1
4	:	1
8	:	1
16	:	1

PAGE
DATE __/__/__

▶ 2:1 →

2 input, 1 output and 1 select line

Select line :- $2^n = 2$ $\quad 2^1 = 2$



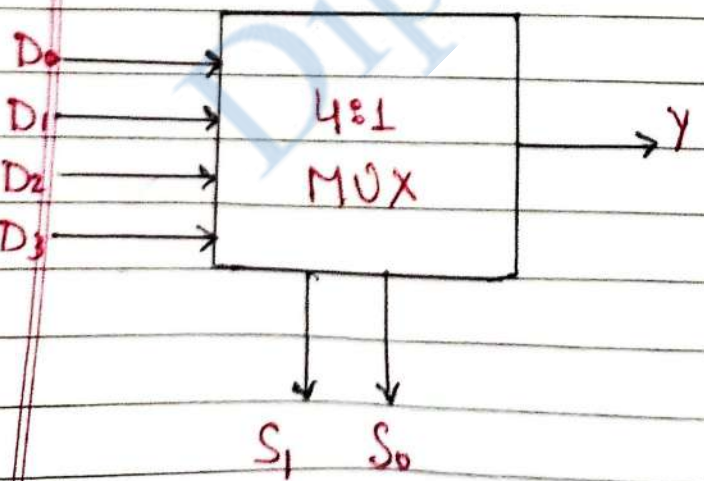
Truth table :-

S_0	Y
0	D_0
1	D_1

▶ 4:1 →

4 input, 1 output and 2 select line.

Select line :- $2^n = 4$ $\quad 2^2 = 4$



Truth table

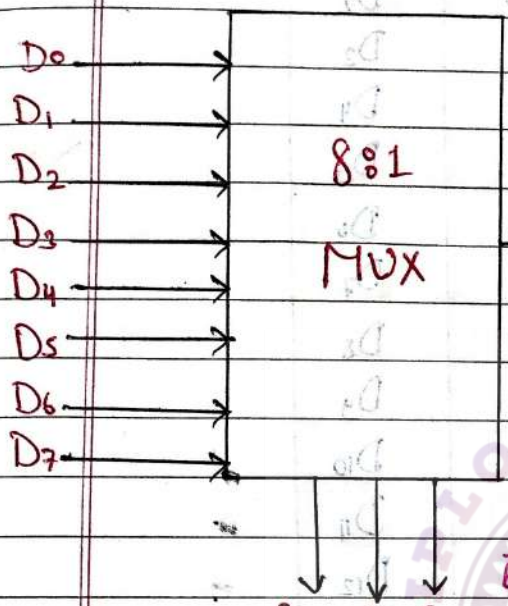
S_1	S_0	Y
0	0	D_0
0	1	D_1
1	0	D_2
1	1	D_3

PAGE_____
DATE__/__/__

8 : 1 →

8 input, 1 output and 3 select line

Select line :~ $2^n = 8$ $\quad 2^3 = 4$



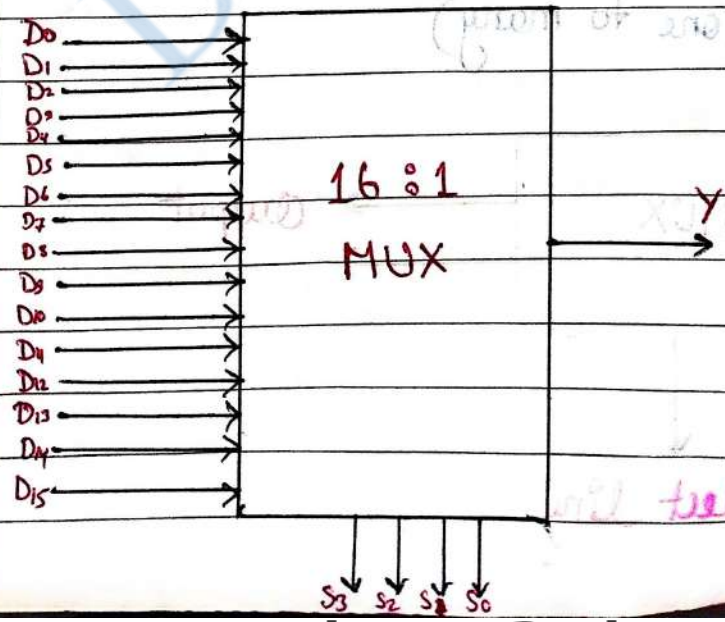
Truth table :~

E	S_2	S_1	S_0	Y
0	0	0	0	D_0
0	0	0	1	D_1
0	0	1	0	D_2
0	0	1	1	D_3
0	1	0	0	D_4
0	1	0	1	D_5
0	1	1	0	D_6
0	1	1	1	D_7

16 : 1 →

16 input, 1 output and 4 select line

Select line :~ $2^n = 16$ $\quad 2^n = 16$



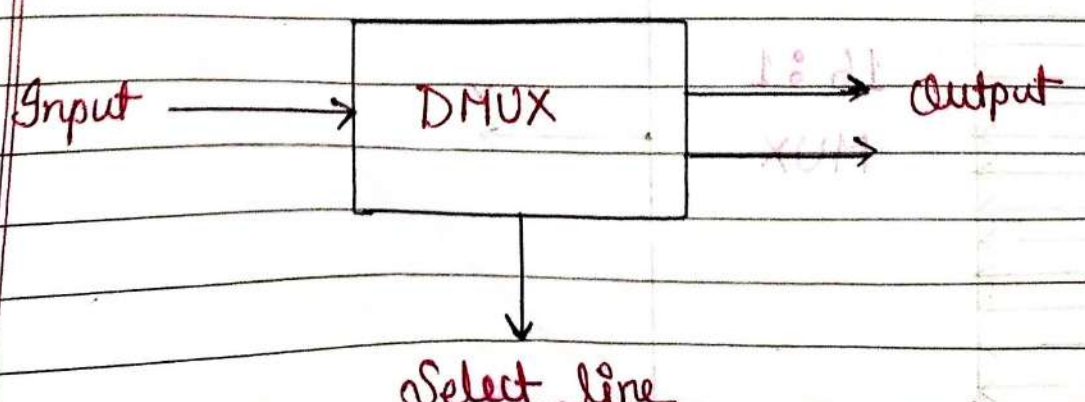
PAGE_____
DATE__/__/__

Truth table :~

S	S_3	S_2	S_1	S_0	Y
0	0	0	0	0	D_0
0	0	0	0	1	D_1
0	0	0	1	0	D_2
0	0	0	1	1	D_3
0	0	1	0	0	D_4
0	0	1	0	1	D_5
0	0	1	1	0	D_6
0	0	1	1	1	D_7
0	1	0	0	0	D_8
0	1	0	0	1	D_9
0	1	0	1	0	D_{10}
0	1	0	1	1	D_{11}
0	1	1	0	0	D_{12}
0	1	1	0	1	D_{13}
0	1	1	1	0	D_{14}
0	1	1	1	1	D_{15}

Demultiplexer (DMUX) : Data distributer :~

(one to many)



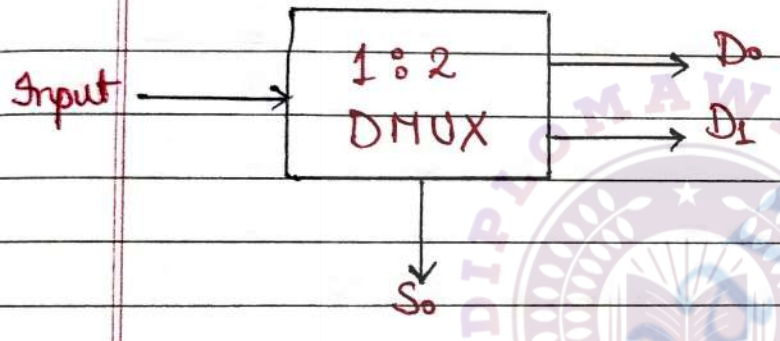
Input		Output
1	:	2
1	:	4
1	:	8
1	:	16

▶ 1 : 2 →

1 input, 2 output and 1 select line.

Select line :- $2^{(n)} = 2$

$2^{(1)} = 2$



Truth table

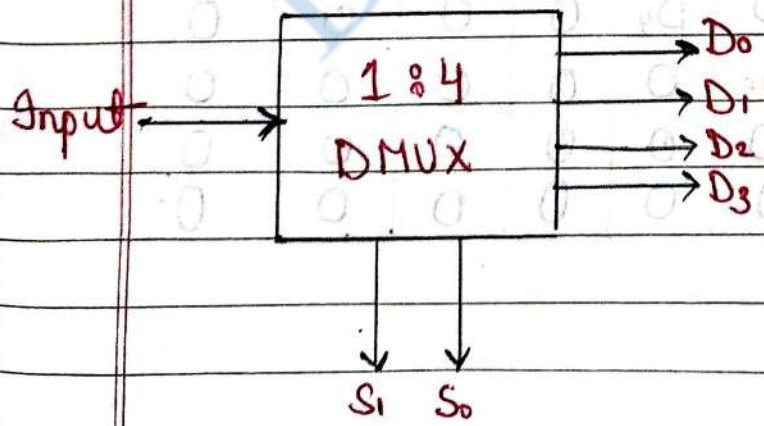
S_0	Y_1	Y_0
0	0	D_0
1	D_1	0

▶ 1 : 4 →

1 input, 4 output and 2 select line

Select line :- $2^{(n)} = 4$

$2^{(2)} = 4$



Truth table

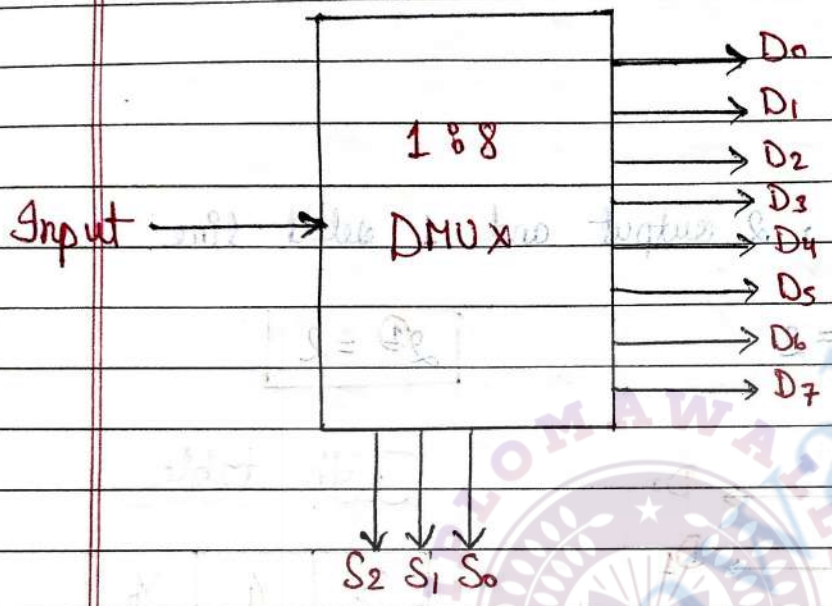
S_1	S_0	Y_3	Y_2	Y_1	Y_0
0	0	0	0	0	D_0
0	1	0	0	D_1	0
1	0	0	D_2	0	0
1	1	D_3	0	0	0

PAGE
DATE __/__/__

1 : 8 →

1 input, 8 output and 3 select line.

Select line :~ $2^{n} = 8$ $\quad 2^{3} = 8$



Truth table :~

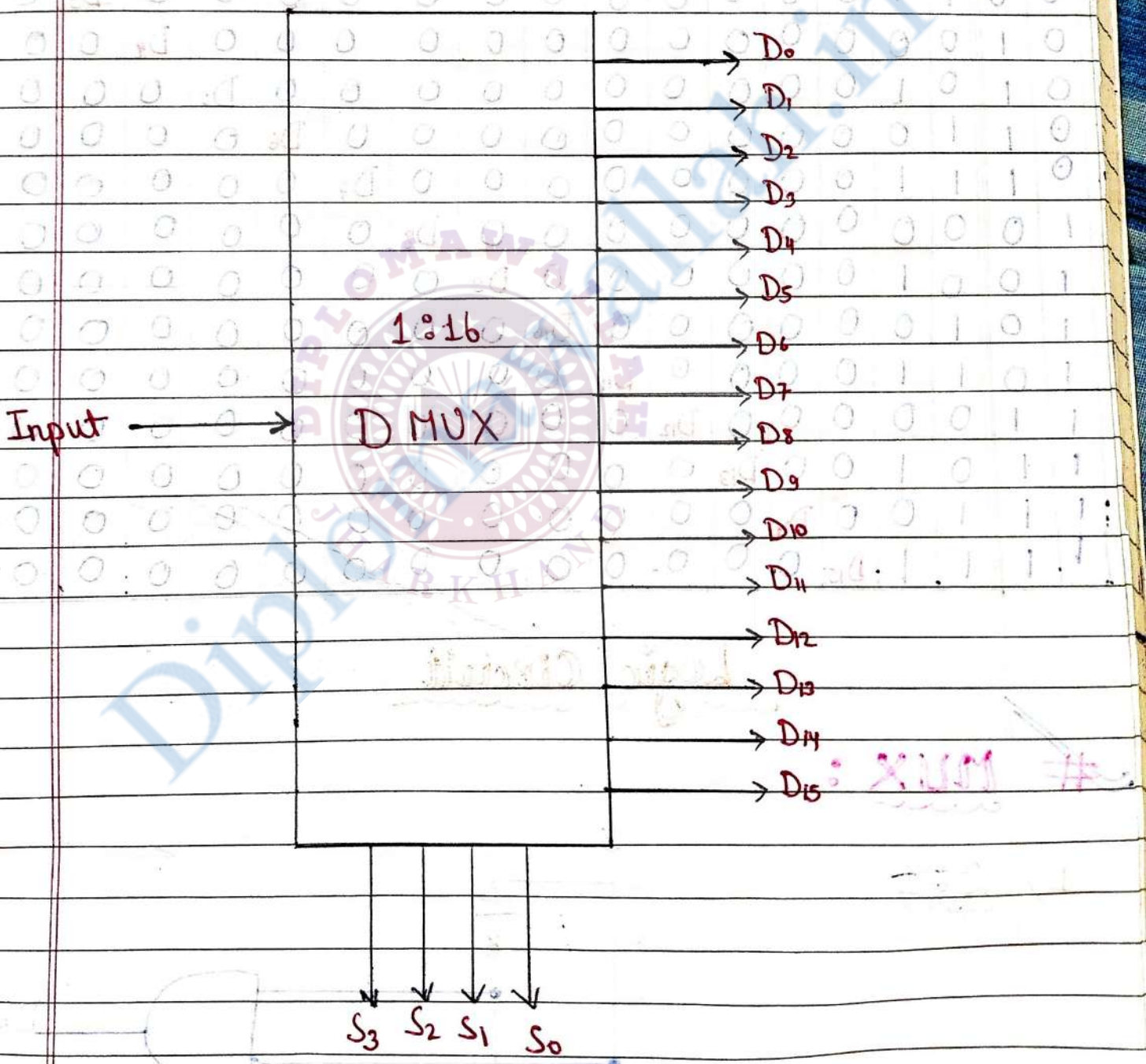
S_2	S_1	S_0	Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1	Y_0
0	0	0	0	0	0	0	0	0	0	D_0
0	0	1	0	0	0	0	0	0	D_1	0
0	1	0	0	0	0	0	0	D_2	0	0
0	1	1	0	0	0	0	D_3	0	0	0
1	0	0	0	0	0	D_4	0	0	0	0
1	0	1	0	0	D_5	0	0	0	0	0
1	1	0	0	D_6	0	0	0	0	0	0
1	1	1	D_7	0	0	0	0	0	0	0

PAGE
DATE __/__/__

1 : 16 →

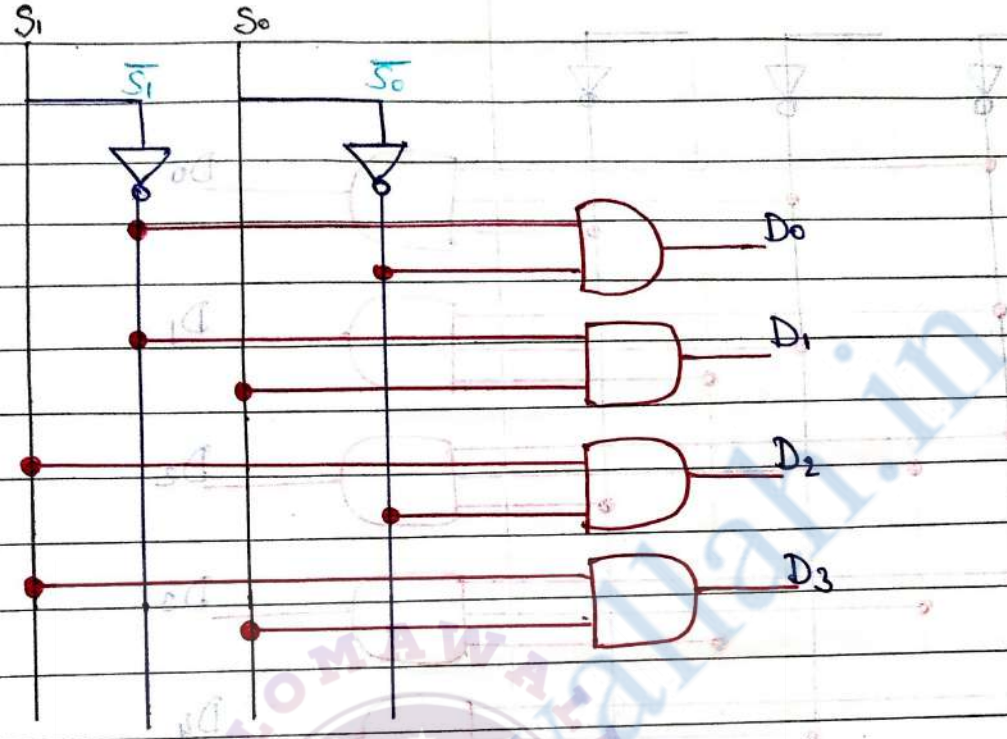
1 input, 16 output and 4 select line.

Select line :- $2^n = 16$ $\quad 2^4 = 16$ $\quad \therefore$



PAGE
DATE / /

2.) 4 : 1



Boolean Expression

D_0	$\overline{S_1}$	$\overline{S_0}$	
D_1	$\overline{S_1}$	S_0	
D_2	S_1	$\overline{S_0}$	
D_3	S_1	S_0	

PAGE_____
DATE__/__/__

Truth table :-

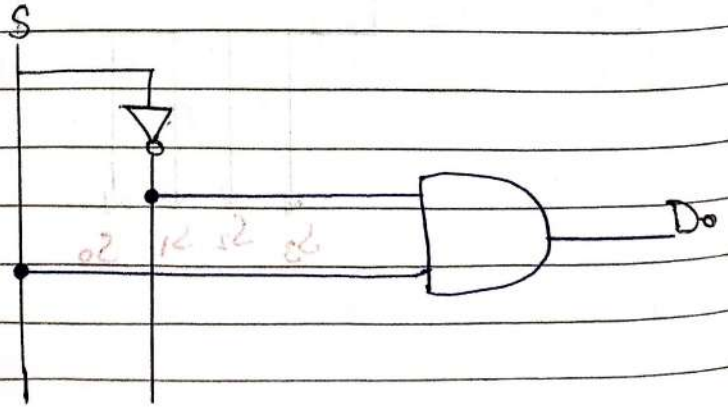
2.) 4

S_0	S_2	S_1	S_0	Y_{15}	Y_{14}	Y_{13}	Y_{12}	Y_{11}	Y_{10}	Y_9	Y_8	Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1	Y_0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	D_0
0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	D_1	0
0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	D_2	0	0
0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	D_3	0	0	0
0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	D_4	0	0	0	0
0	1	0	1	0	0	0	0	0	0	0	0	0	0	D_5	0	0	0	0	0
0	1	1	0	0	0	0	0	0	0	0	0	0	D_6	0	0	0	0	0	0
0	1	1	1	0	0	0	0	0	0	0	0	D_7	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0	D_8	0	0	0	0	0	0	0	0
1	0	0	1	0	0	0	0	0	0	D_9	0	0	0	0	0	0	0	0	0
1	0	1	0	0	0	0	0	0	D_{10}	0	0	0	0	0	0	0	0	0	0
1	0	1	1	0	0	0	0	D_{11}	0	0	0	0	0	0	0	0	0	0	0
1	1	0	0	0	0	0	D_{12}	0	0	0	0	0	0	0	0	0	0	0	0
1	1	0	1	0	0	D_{13}	0	0	0	0	0	0	0	0	0	0	0	0	0
1	1	1	0	0	D_{14}	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	1	1	1	D_{15}	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Logic Circuit :

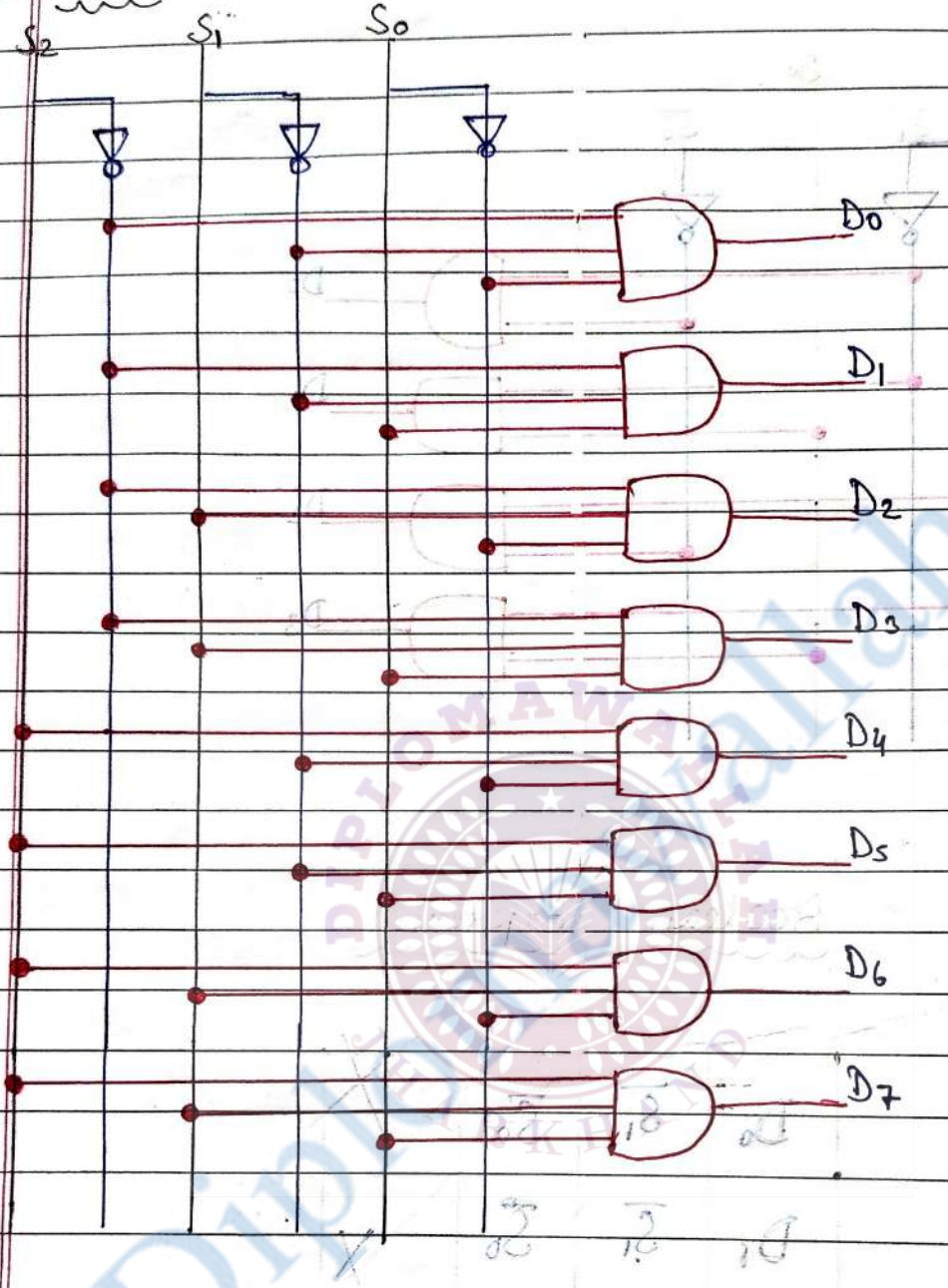
MUX :

1.) 2 : 1



PAGE
DATE __/__/__

3) 8:1

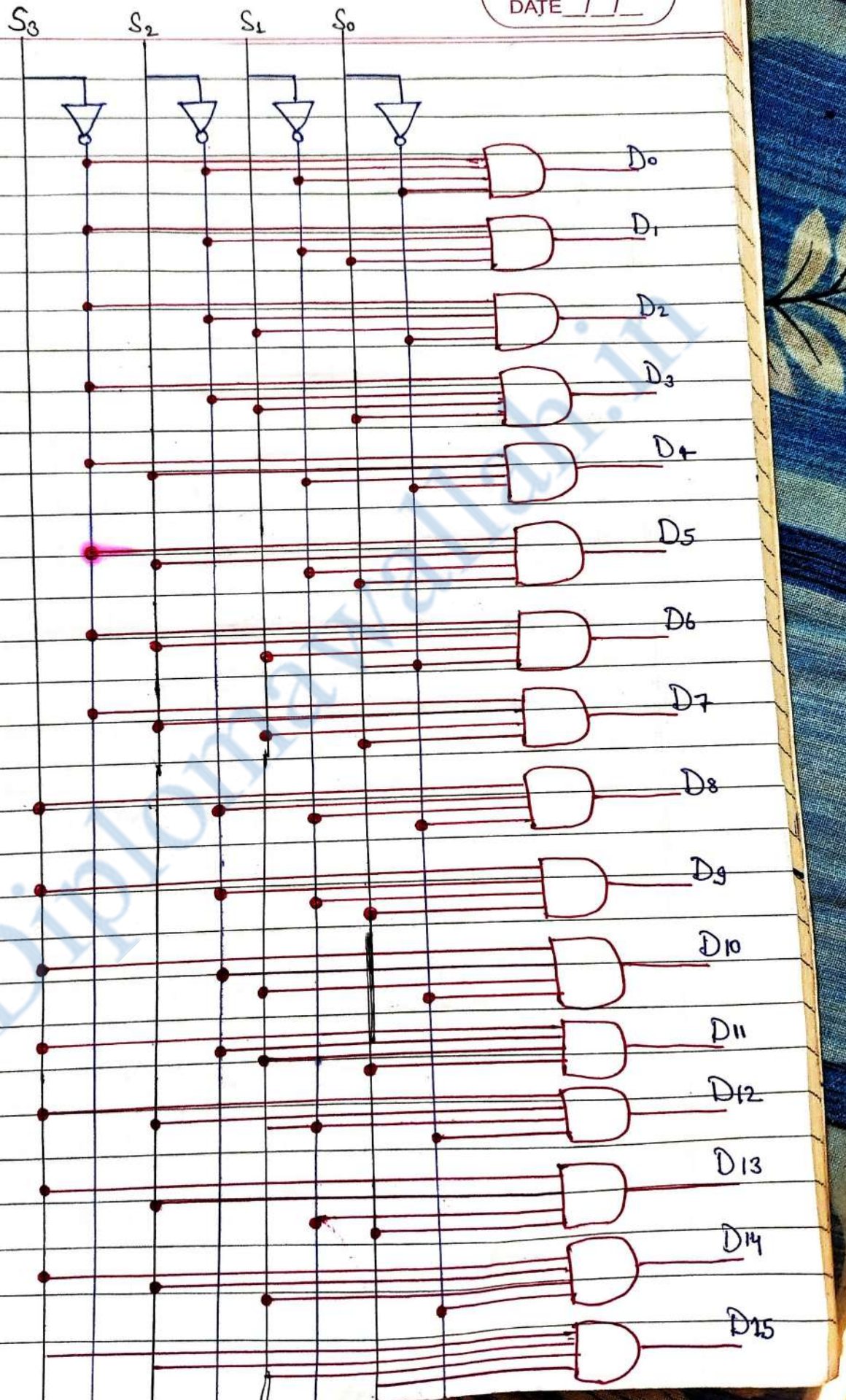


Boolean expression

D_0	$\overline{S}_2$	$\overline{S}_1$	$\overline{S}_0$
D_1	$\overline{S}_2$	$\overline{S}_1$	S_0
D_2	$\overline{S}_2$	S_1	$\overline{S}_0$
D_3	$\overline{S}_2$	S_1	S_0
D_4	S_2	$\overline{S}_1$	$\overline{S}_0$
D_5	S_2	$\overline{S}_1$	S_0
D_6	S_2	S_1	$\overline{S}_0$
D_7	S_2	S_1	S_0

PAGE_____
DATE__/__/__

4.) 16 : 1



PAGE
DATE 1 1

Boolean Expression

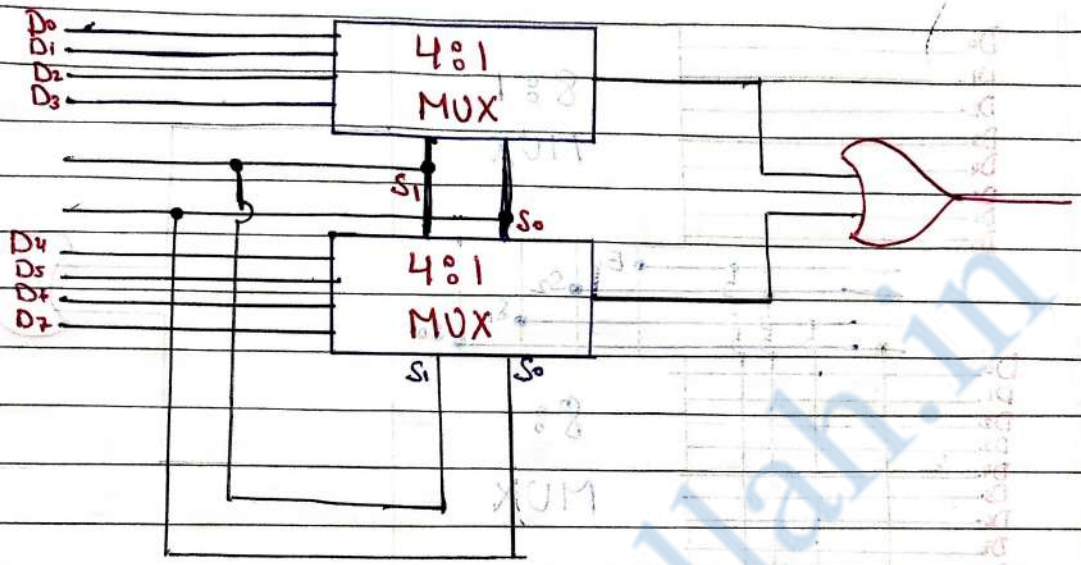
D_0	$\bar{S}_3$	$\bar{S}_2$	$\bar{S}_1$	$\bar{S}_0$
D_1	$\bar{S}_3$	$\bar{S}_2$	$\bar{S}_1$	S_0
D_2	$\bar{S}_3$	$\bar{S}_2$	S_1	$\bar{S}_0$
D_3	$\bar{S}_3$	$\bar{S}_2$	S_1	S_0
D_4	$\bar{S}_3$	S_2	$\bar{S}_1$	$\bar{S}_0$
D_5	$\bar{S}_3$	S_2	$\bar{S}_1$	S_0
D_6	$\bar{S}_3$	S_2	S_1	$\bar{S}_0$
D_7	$\bar{S}_3$	S_2	S_1	S_0
D_8	S_3	$\bar{S}_2$	$\bar{S}_1$	$\bar{S}_0$
D_9	S_3	$\bar{S}_2$	$\bar{S}_1$	S_0
D_{10}	S_3	$\bar{S}_2$	S_1	$\bar{S}_0$
D_{11}	S_3	$\bar{S}_2$	S_1	S_0
D_{12}	S_3	S_2	$\bar{S}_1$	$\bar{S}_0$
D_{13}	S_3	S_2	$\bar{S}_1$	S_0
D_{14}	S_3	S_2	S_1	$\bar{S}_0$
D_{15}	S_3	S_2	S_1	S_0

29/07/24

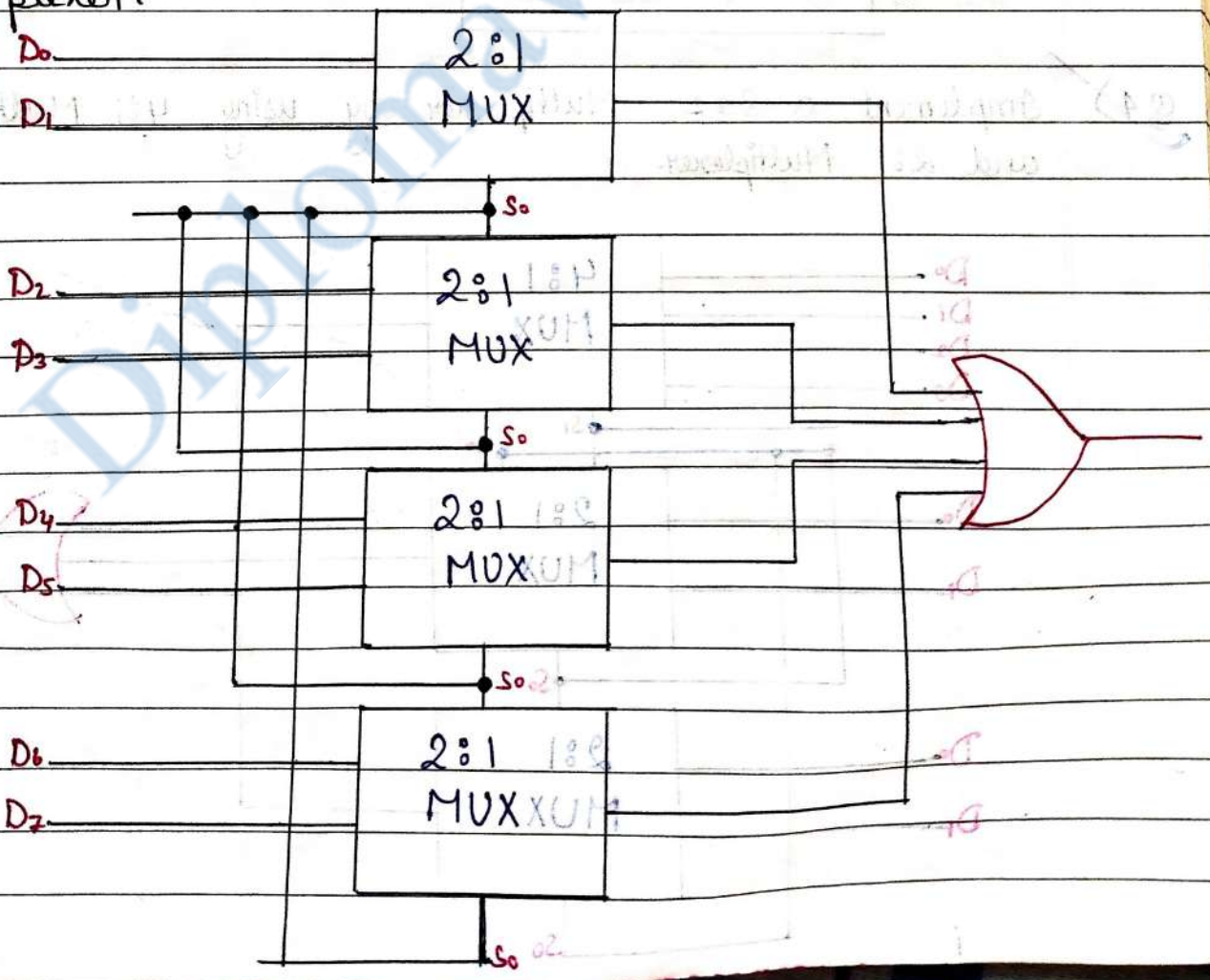
Monday

PAGE
DATE / /

Q1) Implement 8:1 Multiplexer by using two 4:1 multiplexer.



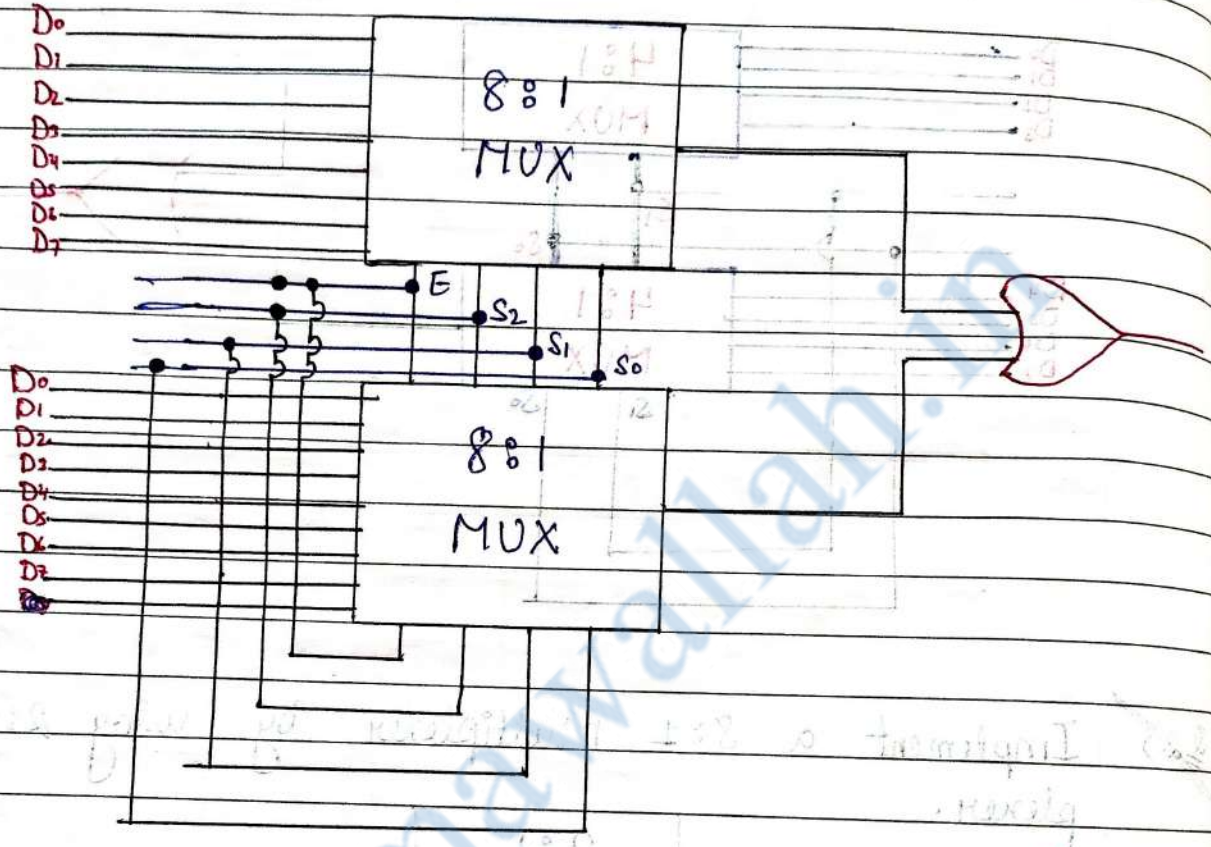
Q2) Implement a 8:1 Multiplexer by using 2:1 multiplexer.



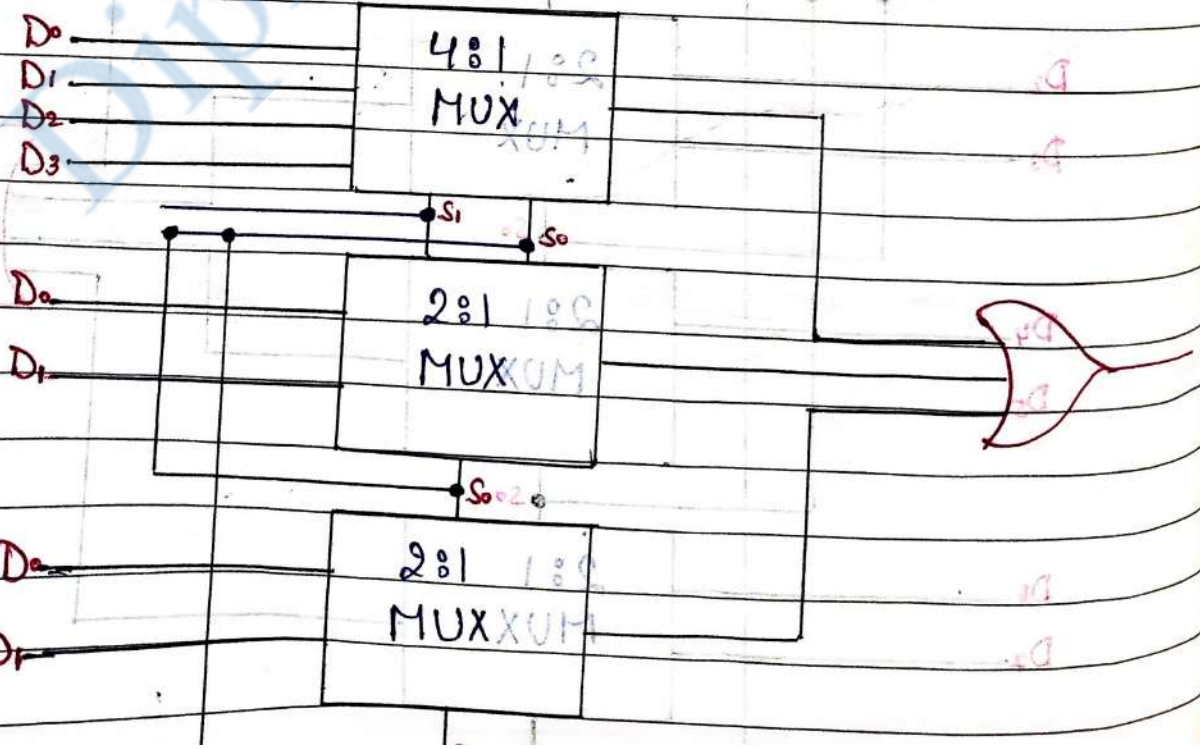
Question bank question

PAGE
DATE / /

Q3 Implement a 16:1 Multiplexer by using two 8:1 Multiplexer IC.



Q4 Implement a 8:1 Multiplexer by using 4:1 Multiplexer and 2:1 Multiplexer.



05/09/24

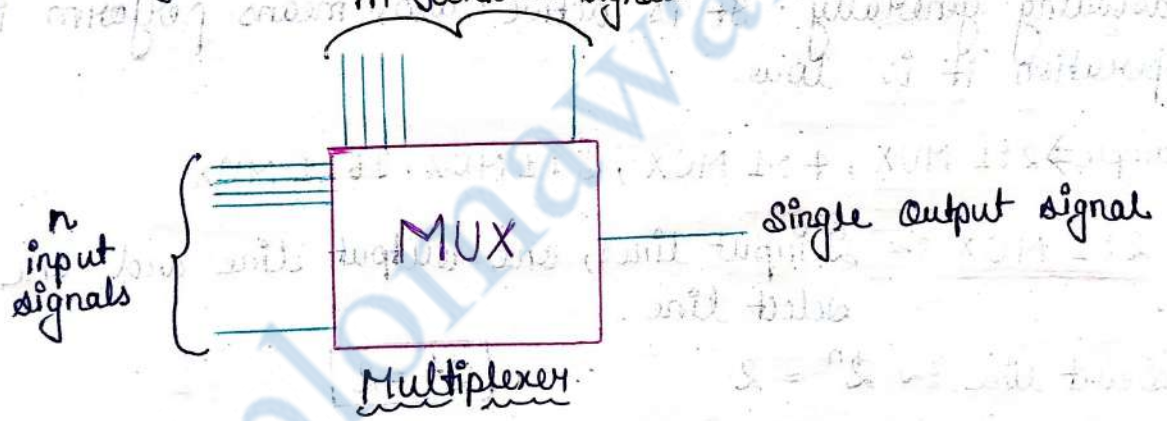
Unit ⇨ 4

Multiplexers & Demultiplexers

1) What is multiplexer? Draw a block diagram with example:- (2015-2017)

Sol^{n}⇒ Multiplexer means 'many into one'. Hence, as the name suggests, a multiplexer is a circuit with many inputs but only one output. With the help of control signals it is possible to steer and guide any input into the output.

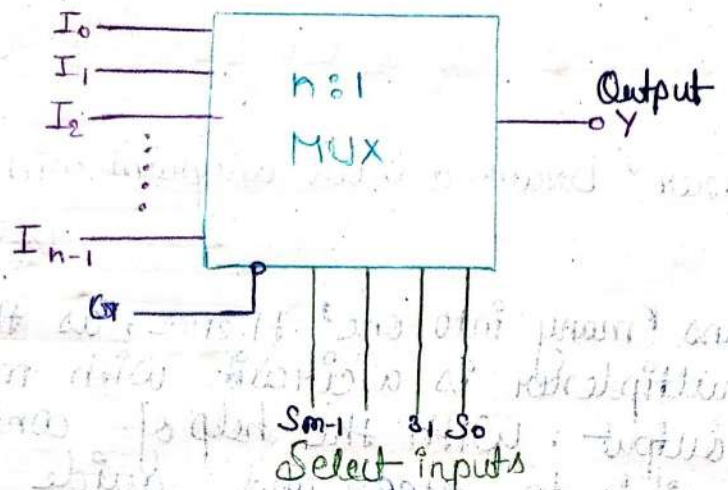
The multiplexer shown in it has n input signals but only one output signal. There are m control signals for steering the required input into the output.



- Multiplexer means 'many into one'.
- MUX has several data input lines a single output line..
- The selection of a particular input line is controlled by a set of selection lines.
- Normally there are 2^n input lines and n-selection lines.
- It is a special combinational circuit that is one of the most widely used standard circuit in digital design.

INPUT	:	OUTPUT
2	:	1
4	:	1
8	:	1
16	:	1

General Block diagram for n:1 multiplexer.....



$2^m - n$

m – Number of select lines

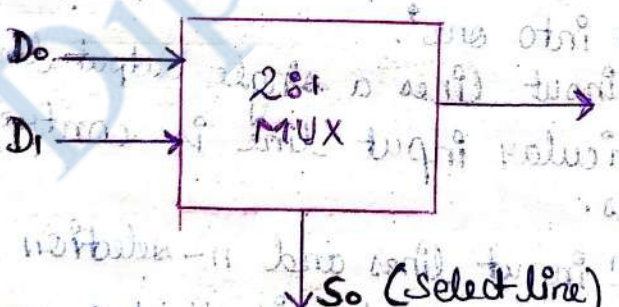
n – Number of input lines

A stable (enable input) is active low input. It helps in cascading generally. It is active low, means perform its operation it is low.

Example ⇒ 2:1 MUX, 4:1 MUX, 8:1 MUX, 16:1 MUX

① 2:1 MUX :- 2 input lines, one output line and one select line.

Select line :- $2^n = 2$ $\boxed{2^1 = 2}$

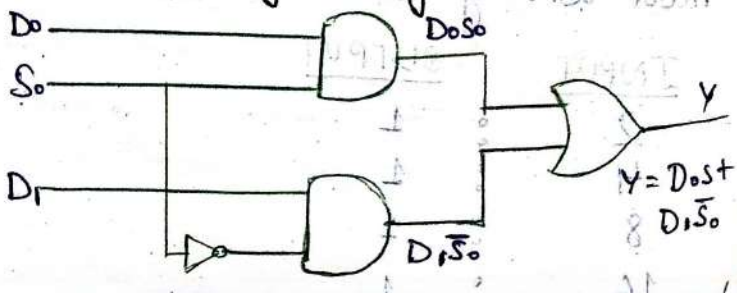


Logic equation $Y = D_0S_0 + D_1\bar{S_0}$

Truth table :-

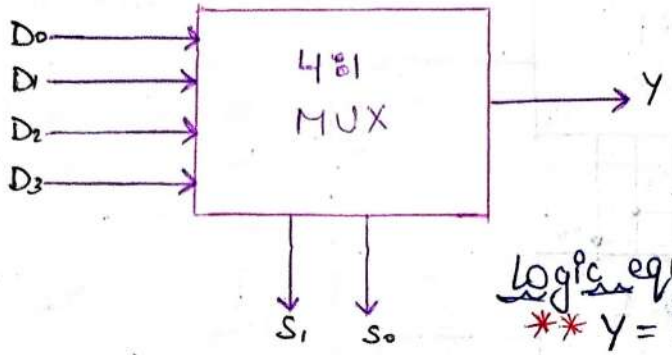
S_0	Y
0	D_0
1	D_1

Logic diagram



② 4:1 MUX :- 4 input lines, 2 select lines and one output line.

Select line :- $2^n = 4$ $\boxed{2^2 = 4}$



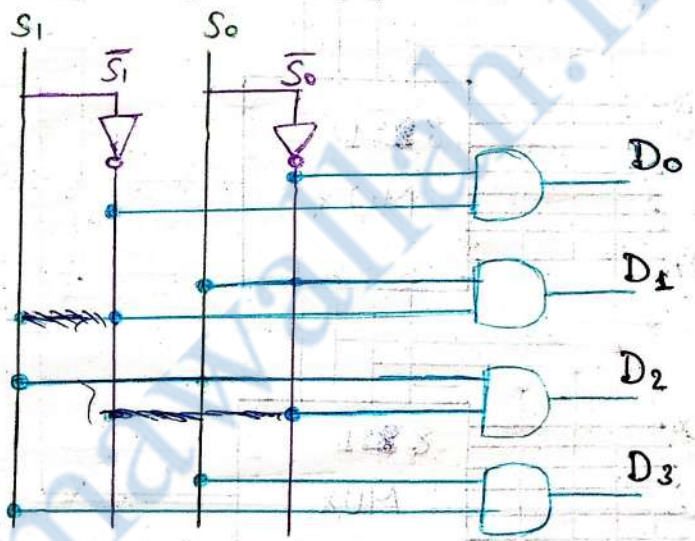
Logic equation :

** $Y = D_0\bar{S_0}\bar{S_1} + D_1S_0\bar{S_1} + D_2\bar{S_0}S_1 + D_3S_0S_1$

Truth table :

S_1	S_0	Y
0	0	D_0
0	1	D_1
1	0	D_2
1	1	D_3

Logic diagram



Same as 8:1 and 16:1, which is write in college copy.....

2) Draw 4:1 multiplexer using logic gates.

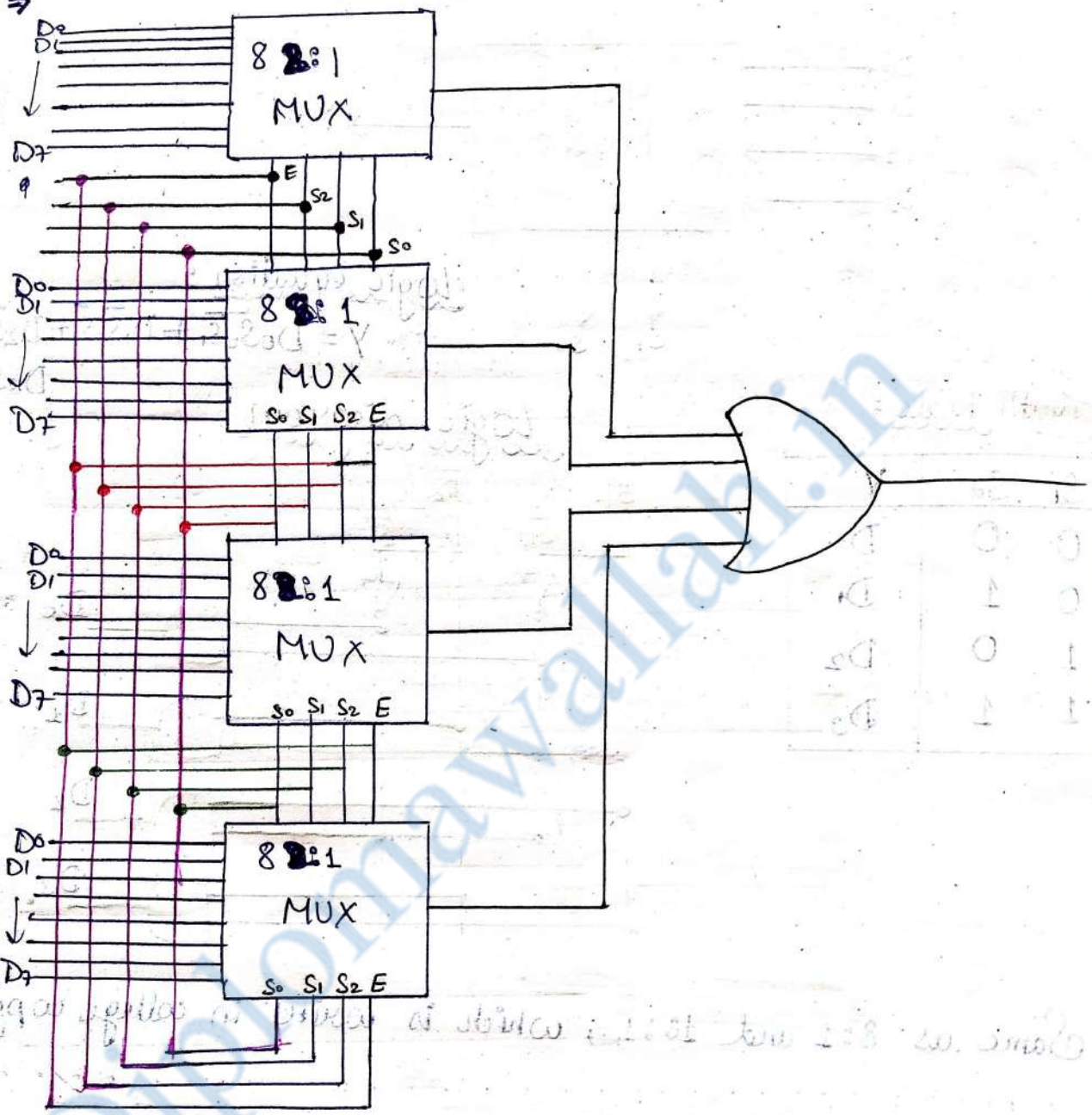
Sol^n ⇒ Same as above first we have to draw truth table then block diagram of 4:1 mux then logic diagram which are shown in the above figure...

Logic diagram of 4:1 Multiplexer Truth table

Inputs			Outputs			
E	S_1	S_0	Y_3	Y_2	Y_1	Y_0
0	0	0	0	0	0	D_0
0	0	1	0	0	D_1	0
0	1	0	0	D_2	0	0
0	1	1	D_3	0	0	0

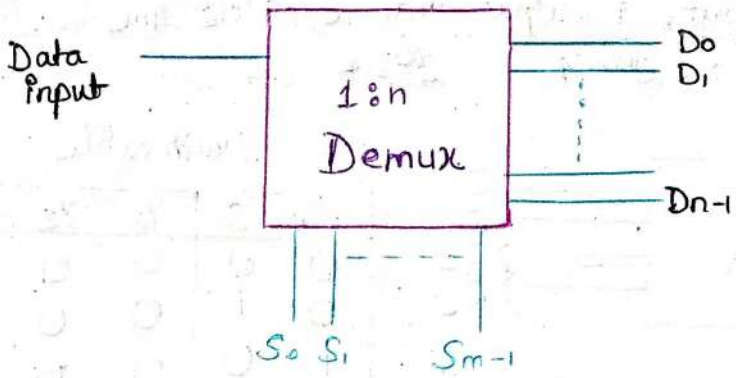
3) Design a 32:1 multiplexer using four 8:1 multiplexers?

Soln⇒



4) Define de-multiplexer. Draw generalized block diagram in 1:n de-multiplexer. (2019)

Soln⇒ A demultiplexer performs the reverse operation of a multiplexer i.e. it receives one input and distributes it over several outputs. It has only one input, n outputs, m select lines inputs. At a time only one output line is selected by the select lines and the input is transmitted to the selected output line. A de-multiplexer is equivalent to a single pole multiple way switch as shown in fig below.



Demultiplexers comes in multiple variations.

- 1:2 demultiplexer
- 1:4 demultiplexer
- 1:16 demultiplexer
- 1:32 demultiplexer

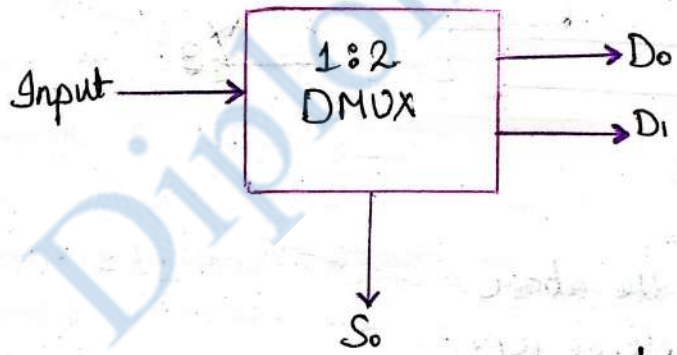
- Demultiplexer means one to many.

The demultiplexer performs the reverse operation of a multiplexer. It accepts a single input and distributes it over several outputs...

Examples:- 1:2 DeMUX, 1:4 DeMUX, 1:8 DeMUX, 1:16 DeMUX

① 1:2 DeMUX :- 1 input, 2 output and 1 select line.

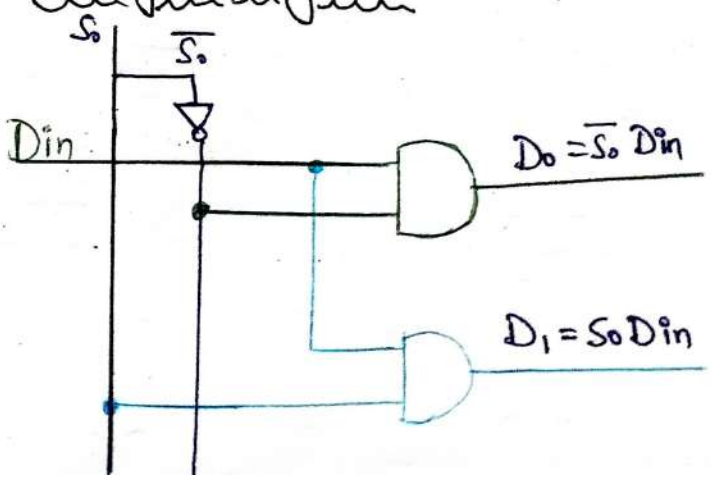
Select line :- $2^n = 2$ $\boxed{2^1 = 2}$



Truth table

Inputs			Outputs	
Din	E	S0	D1	D0
1	1	0	0	1
		1	1	0
0	1	0	1	0
		1	0	1

Logic diagram

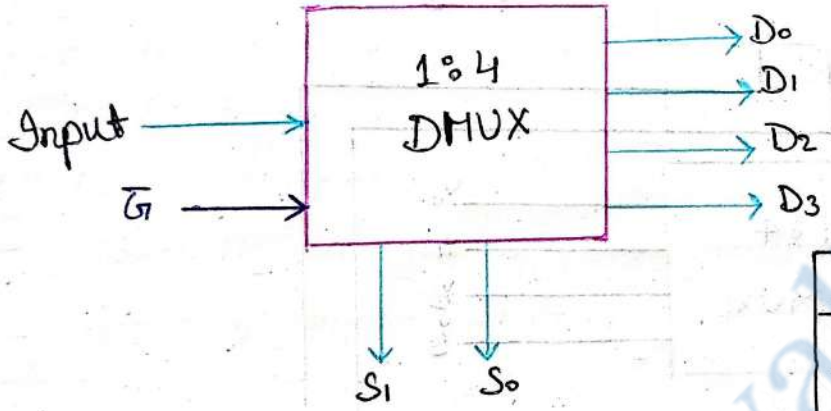


5) Draw the circuit diagram of 1 to 4 line de multiplexer and explain its working.

OR

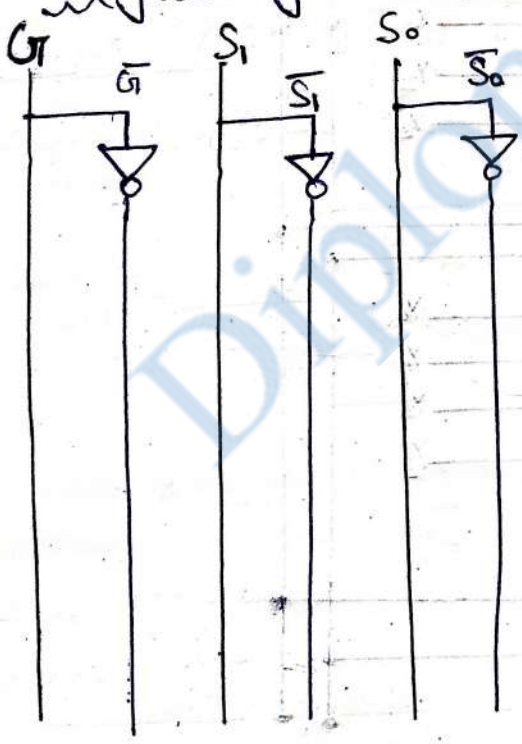
Write truth table for 1:4 demultiplexer. Implement 1:4 demultiplexer using gates....

Soln ⇒ Block diagram of 1:4 Demultiplexer.....



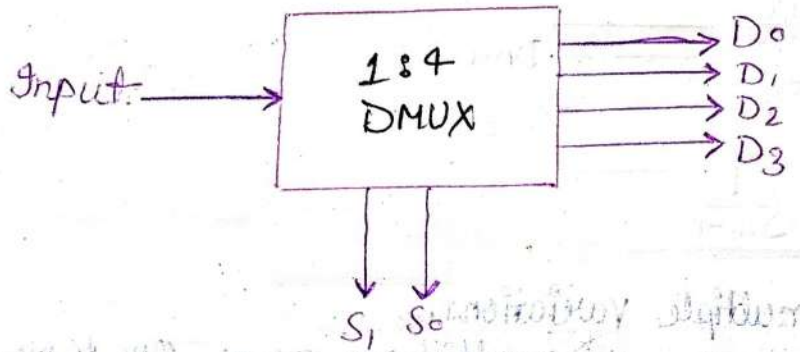
S_1	S_0	Y_3	Y_2	Y_1	Y_0
0	0	0	0	0	D_0
0	1	0	0	D_1	0
1	0	0	D_2	0	0
1	1	D_3	0	0	0

Logic diagram



② 1:4 DMUX :~ 1 input, 4 output and 2 select line

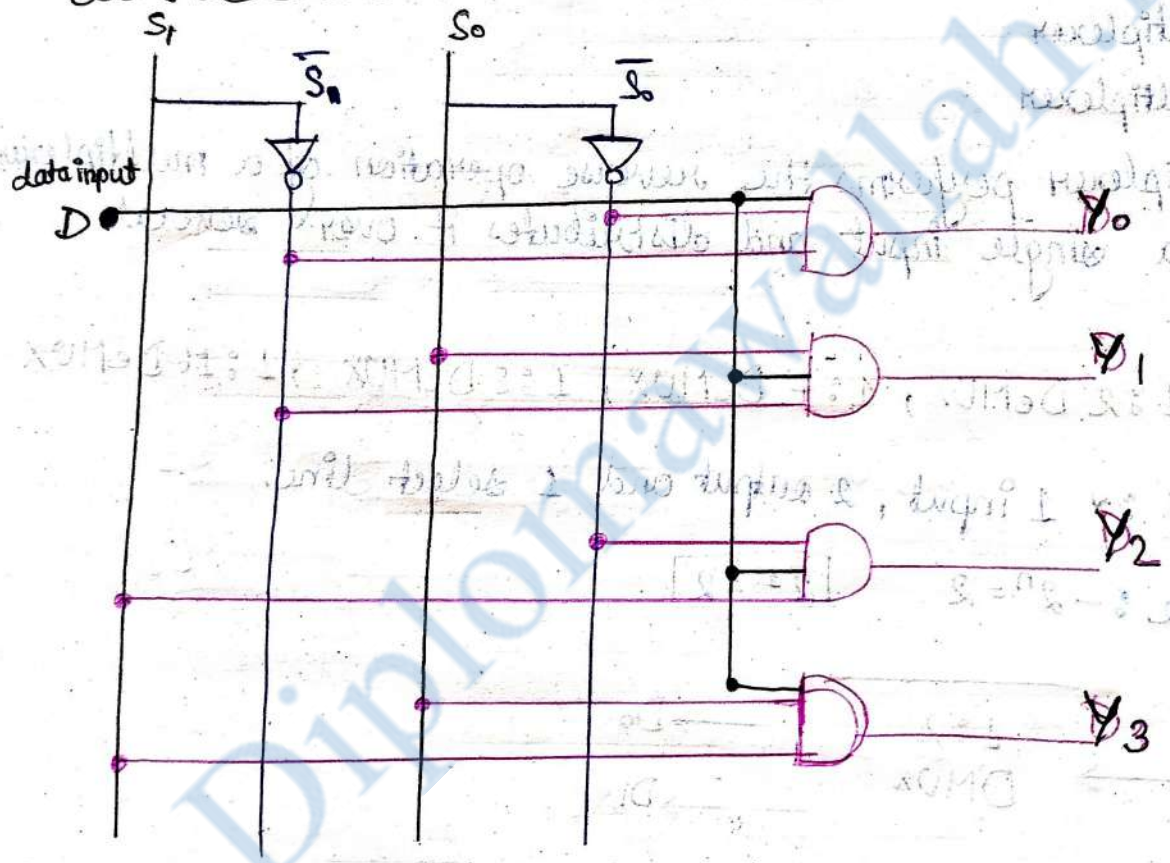
Select line :- $2^n = 4$ $2^2 = 4$



Truth table

S_1	S_0	Y_3	Y_2	Y_1	Y_0
0	0	0	0	0	D_0
0	1	0	0	D_1	0
1	0	0	D_2	0	0
1	1	D_3	0	0	0

Logic circuit



③ 1:8 DMUX

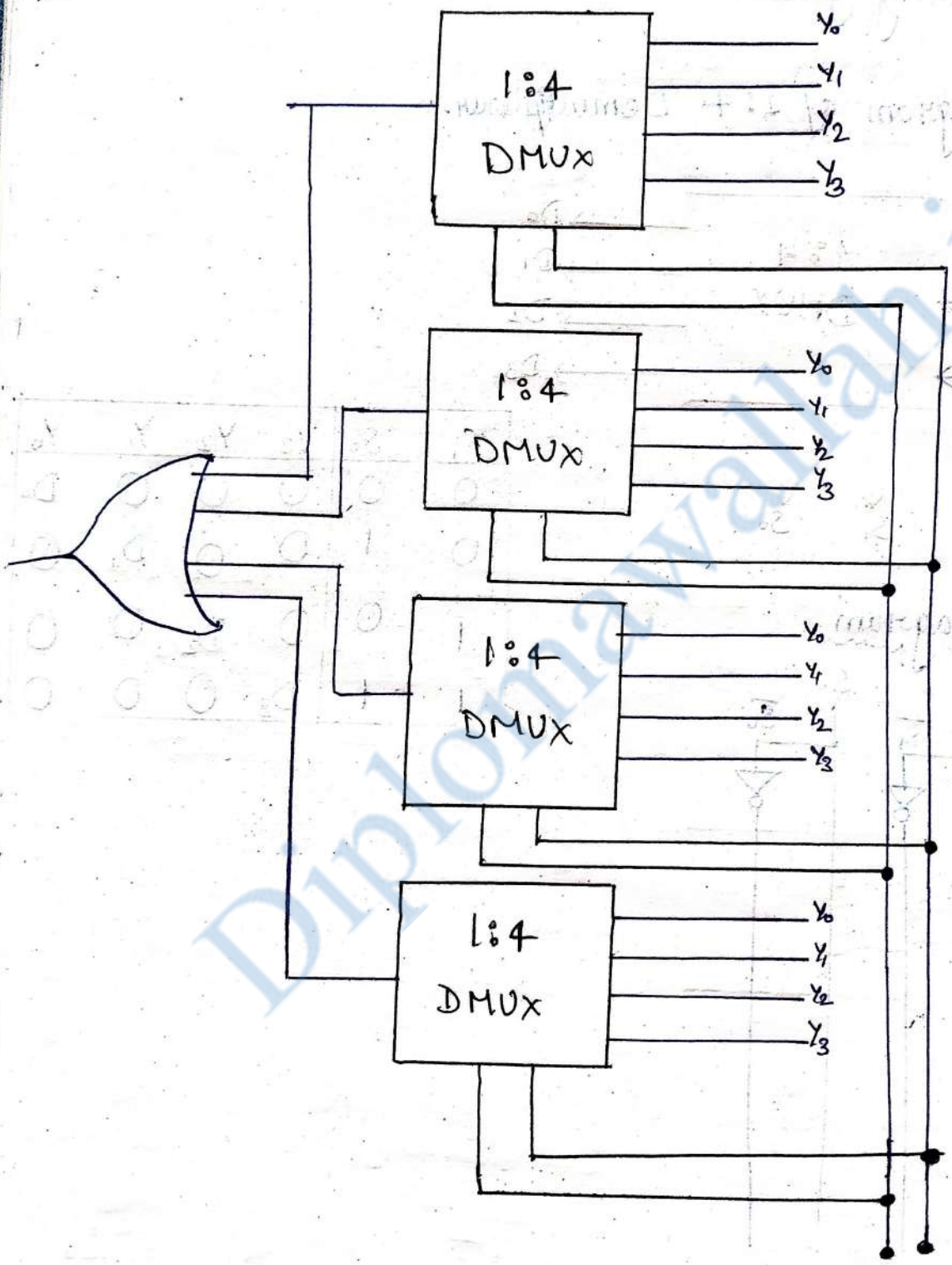
④ 1:16 DMUX is same as the above written in college copy.

6.) Implement a 1:16 demultiplexer using 1:8 demultiplexers?

Soln ⇒ Answer on college copy. . . . . ---

7.) Implement a 1:16 demultiplexer using 1:4 demultiplexers.

Soln ⇒



6.) Implement a 1:16 demultiplexer using 1:8 demultiplexers?

Soln ⇒