10/07/24

Unit - 3

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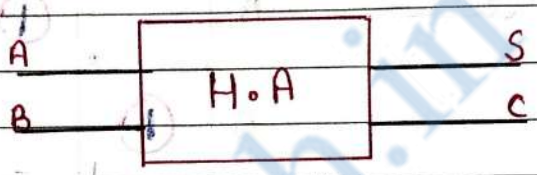
Arithmetic Circuits

Half Adder

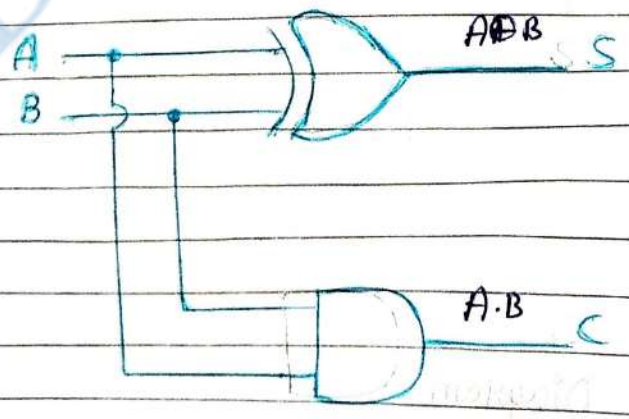


Block diagram

2 input - 2 output

INPUT		OUTPUT	
A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1
		↓ EX-OR Gate	↓ AND Gate

* Logic Circuit Diagram (H.A)



Logic diagram

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* Find the Boolean expression of sum and carry by using k-map method.

Sum :~

B \ A	$\bar{A}$	A
$\bar{B}$	0	(1) 2
B	(1) 1	3

$\Rightarrow A\bar{B} + \bar{A}B$

$A \oplus B$

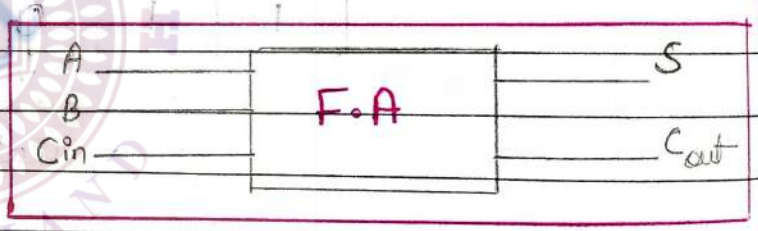
Carry :~

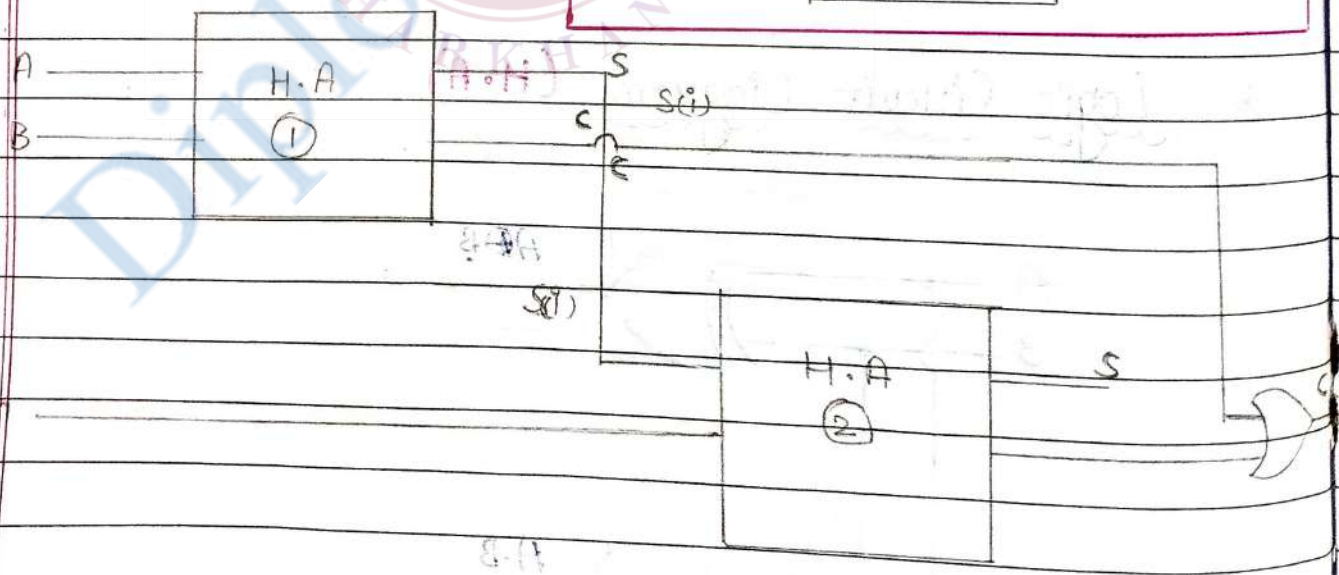
B \ A	$\bar{A}$	A
$\bar{B}$	0	2
B	(1) 1	3

$\Rightarrow AB$

$\Rightarrow A\bar{B} + \bar{A}B + AB$

Full Adder





Block Diagram

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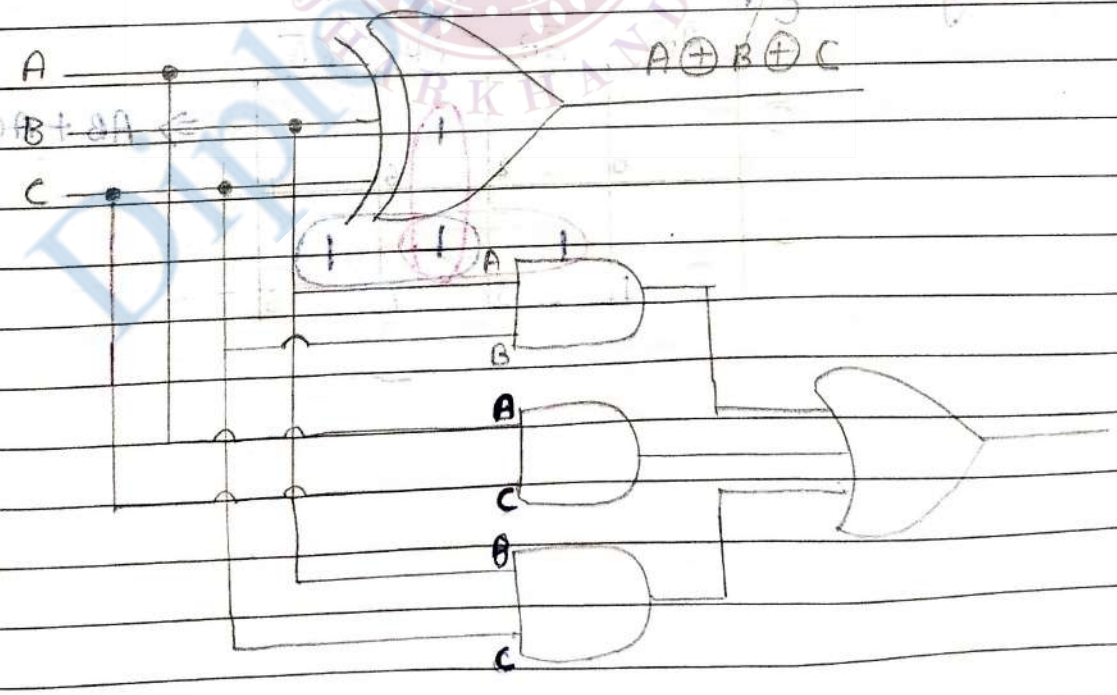
* Truth table :~

A	B	Cin	S	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Homework

1. Draw a logic diagram of Full Adder and find expresions of sum and carry by using k-map method.

Full Adder



Logic diagram

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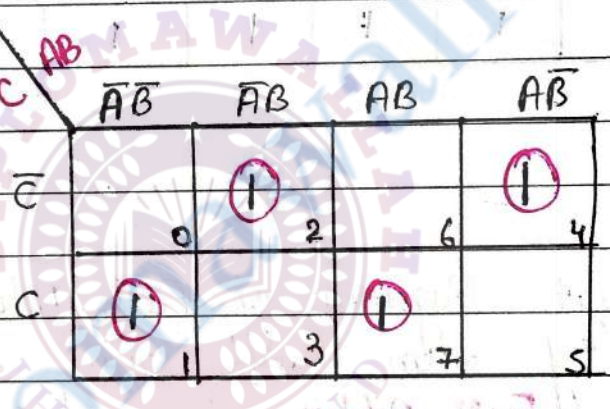
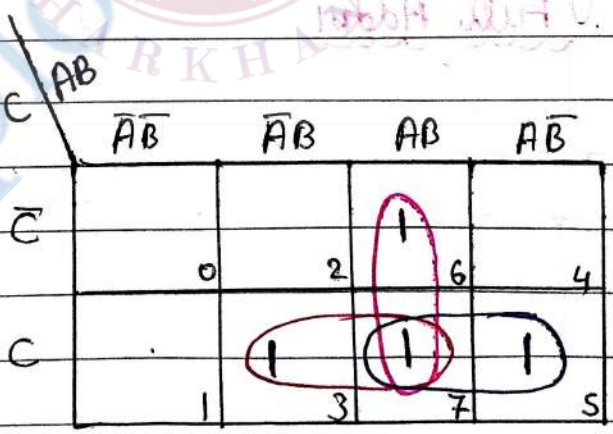
A	B	C	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Sum :~ $2^3 = 8$



$\Rightarrow \bar{A}\bar{B}C + \bar{A}B\bar{C} + ABC + A\bar{B}\bar{C}$

Carry :~



$\Rightarrow AB + AC + BC$

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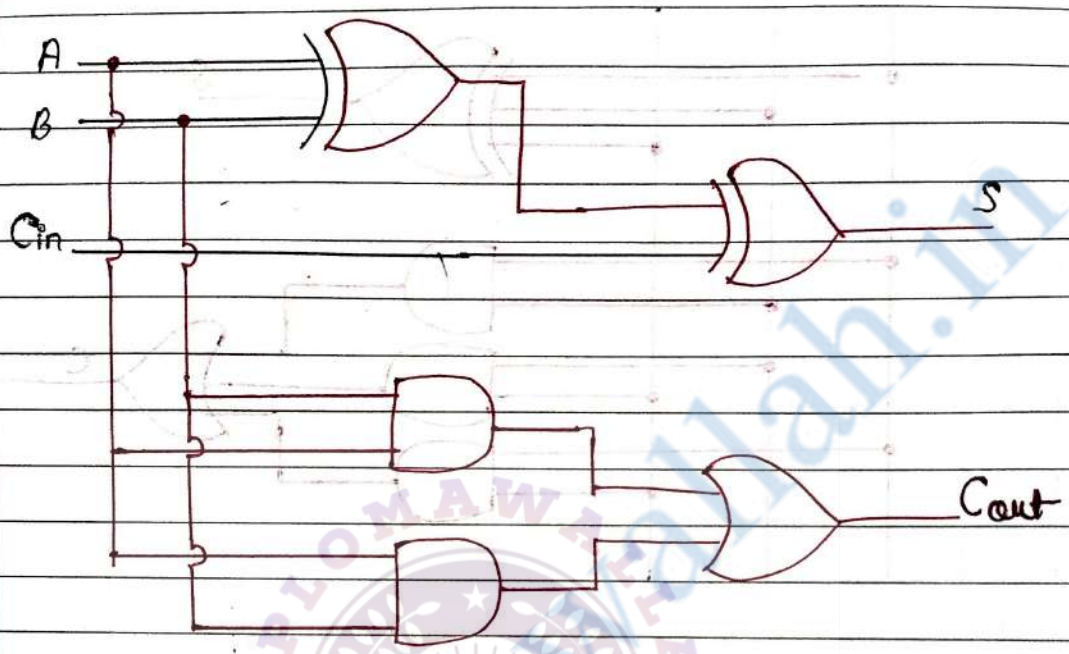
Two Half Adder = Full Adder

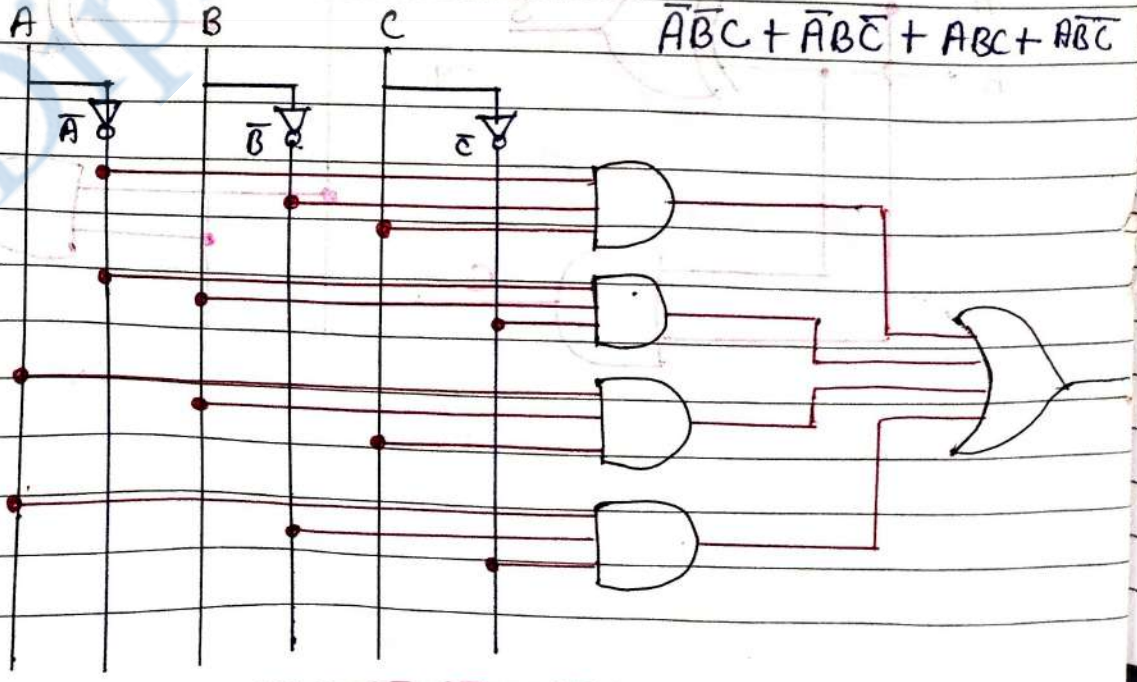


Logic diagram

11/07/24 Thursday

Types of circuit :-

(i) Combinational circuit
(ii) Sequential circuit



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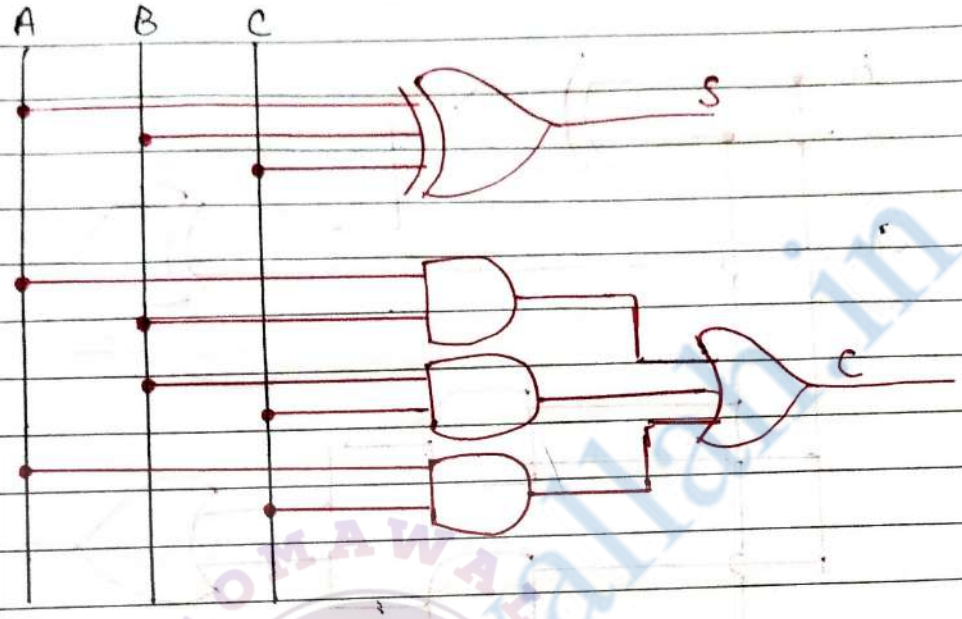
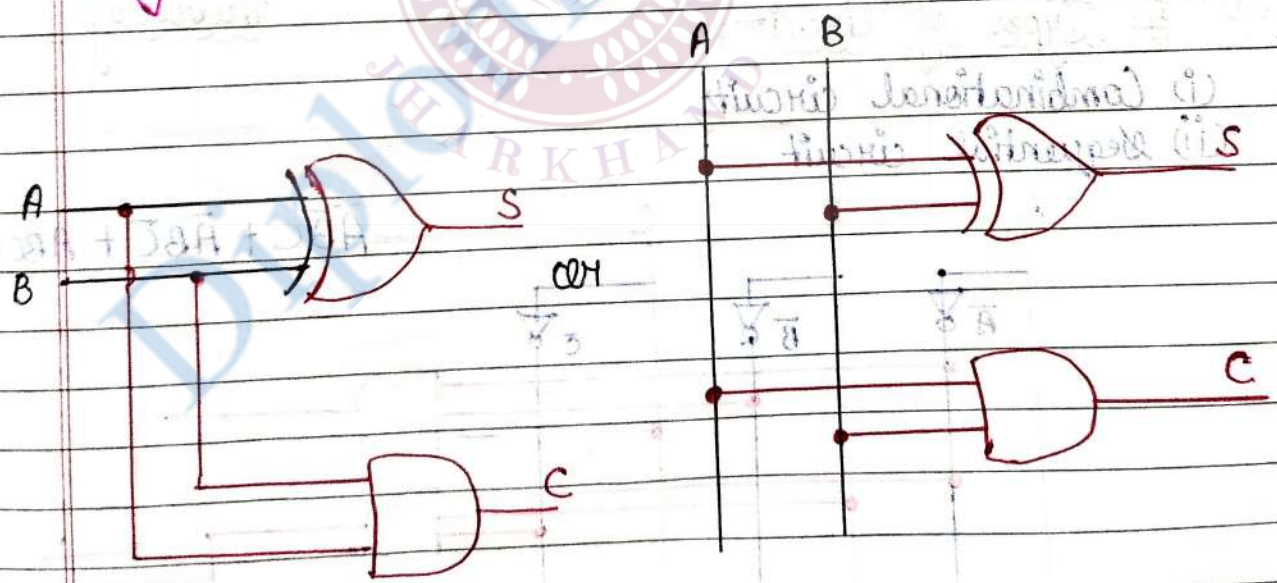
Full Adder Logic diagram



Half Adder Logic diagram



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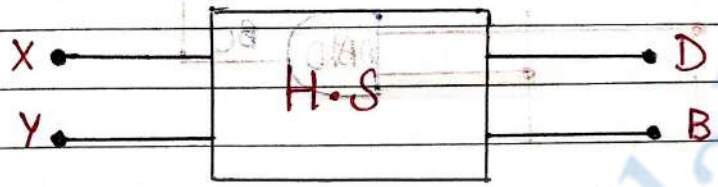
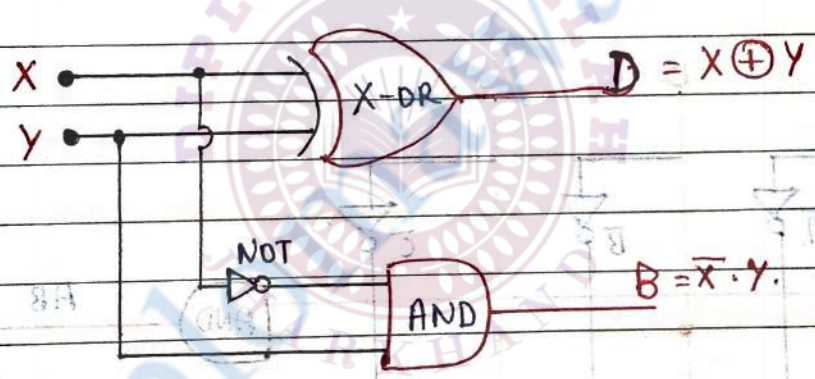
Half Subtracter

2 input — 2 output
↓ ↓
X, Y D :~ Difference
B :~ Borrow



Block diagram



X me NOT gate isliye X̄. Y me AND gate isliye simply Y.

logic diagram

* Half-subtracter truth table :~

X	Y	D	B
0	0	0	0
0	1	1	1 → Borrow
1	0	1	0
1	1	0	0

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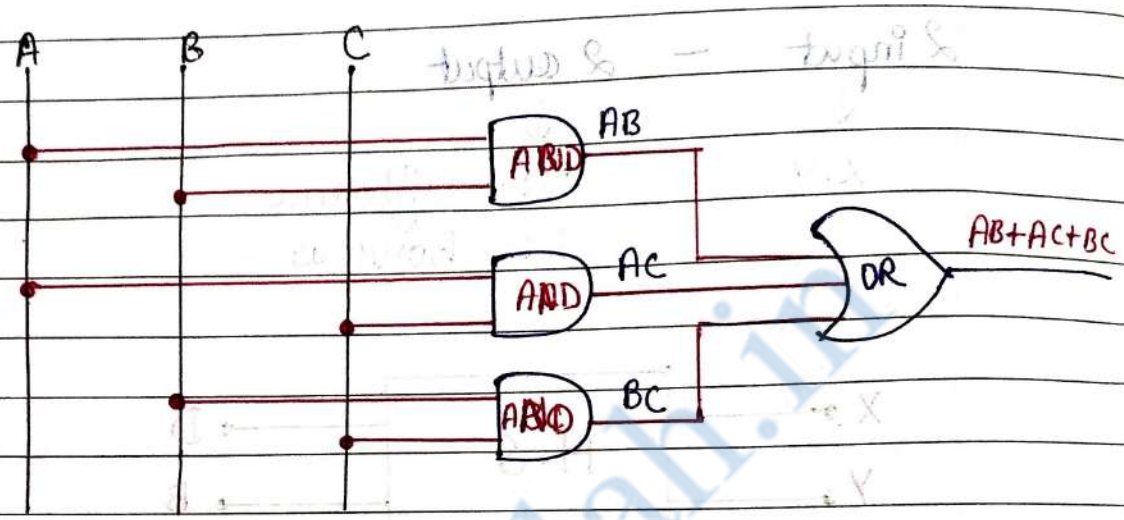
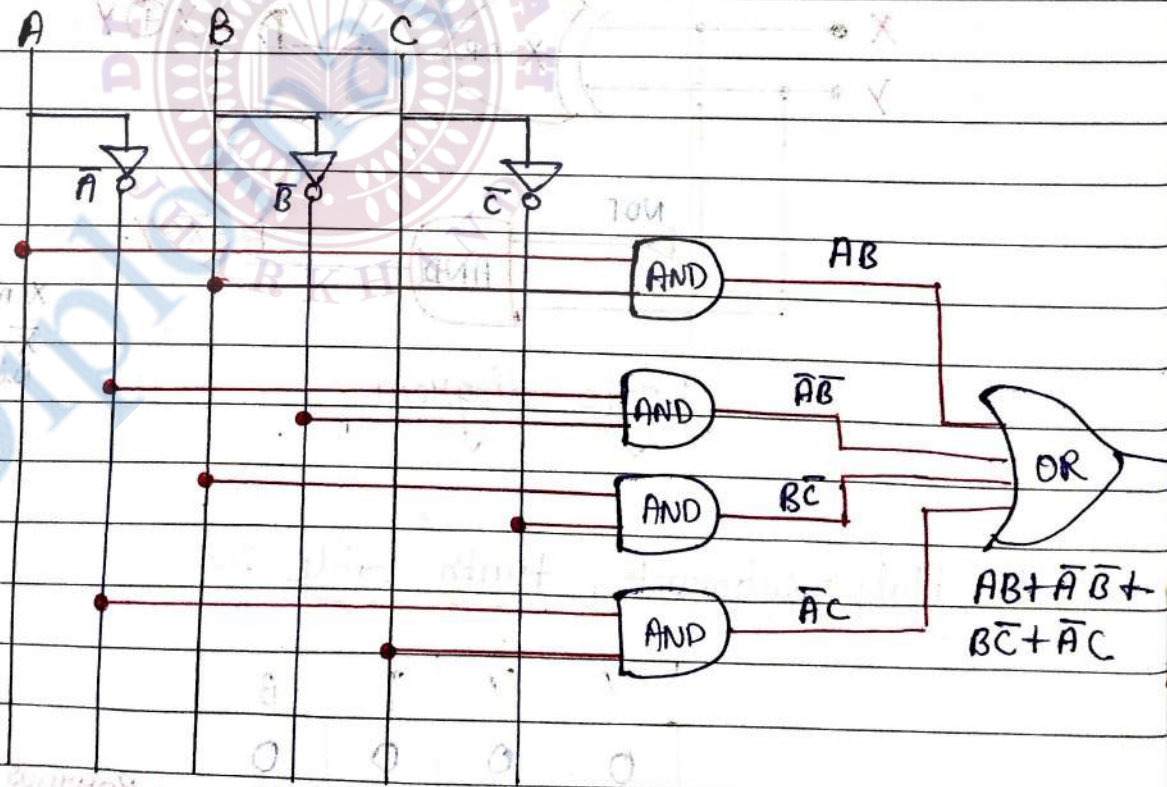
Q.1. Solve this $AB + AC + BC$



Q.2. Solve this $AB + \bar{A}\bar{B} + B\bar{C} + \bar{A}C$



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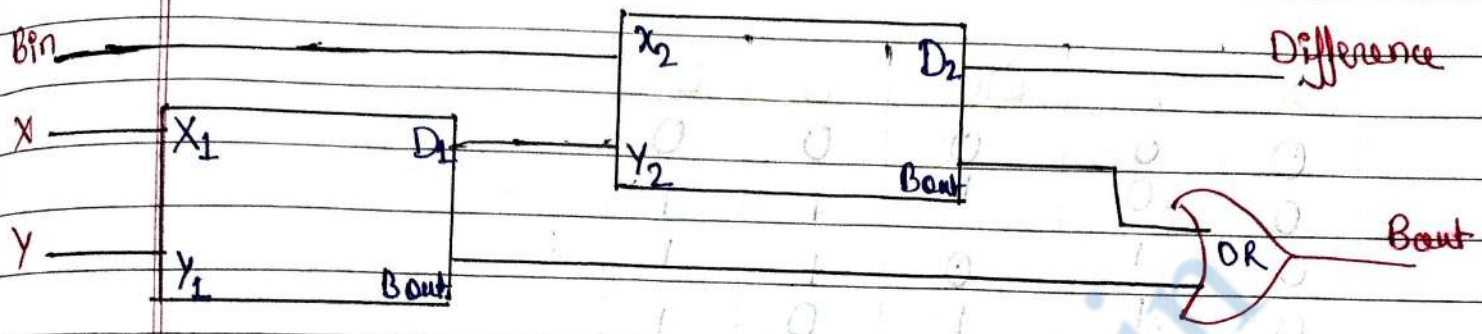
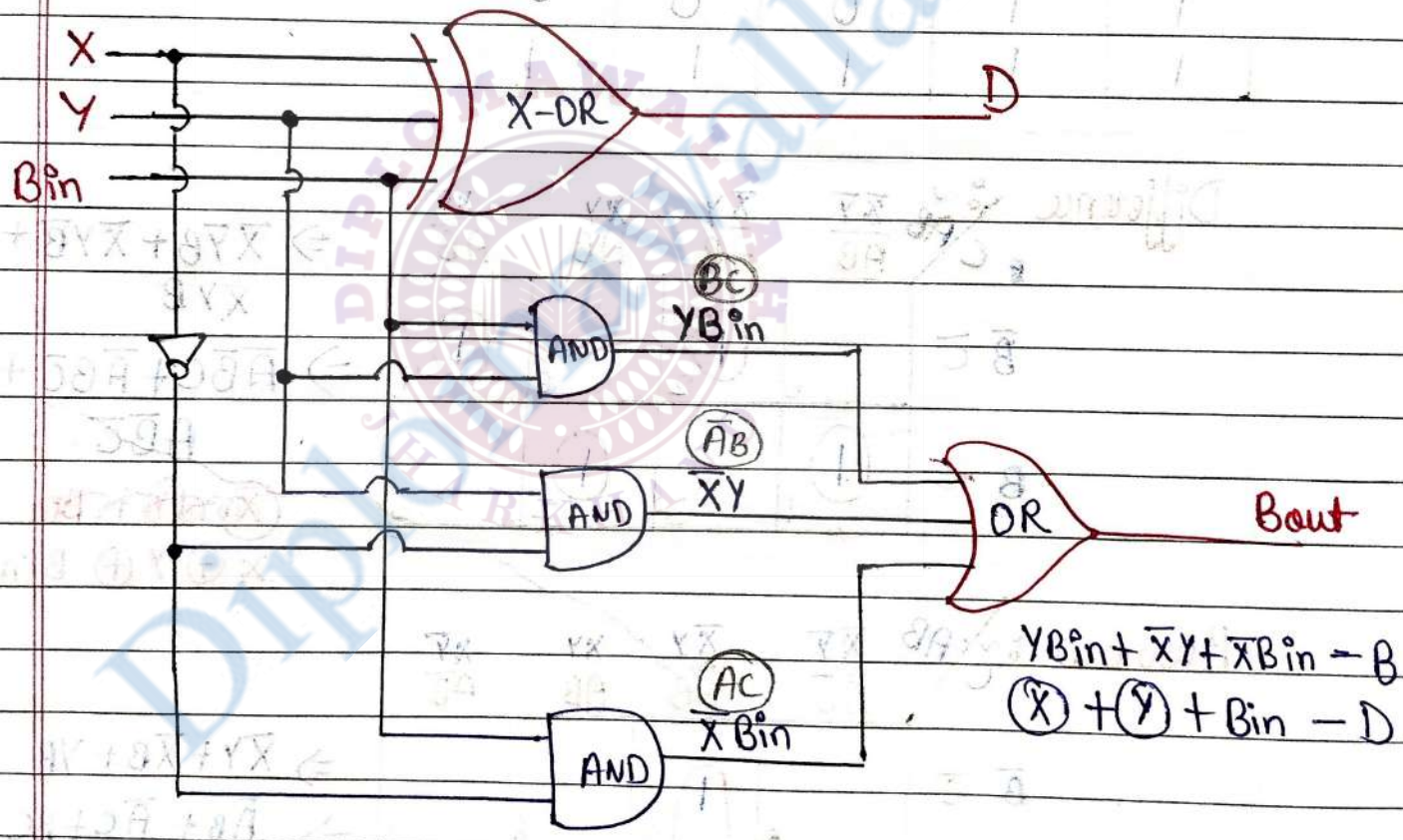
Full Subtracter



Block diagram



Logic diagram

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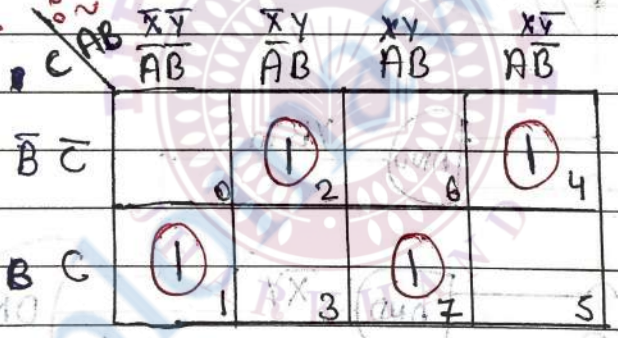
* Full Subtracter truth table:-

X	Y	Bin	D	B
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

Difference :-



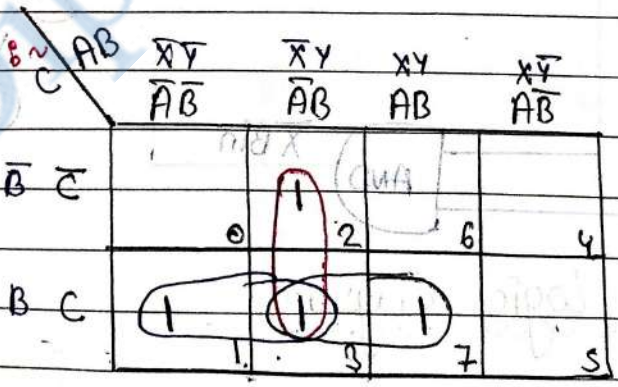
$\Rightarrow \bar{X}\bar{Y}B + \bar{X}Y\bar{B} + X\bar{Y}\bar{B} + XYB$

$\Rightarrow \bar{A}\bar{B}C + \bar{A}B\bar{C} + AB\bar{C} + ABC$

~~$X \oplus Y \oplus Bin$~~

$X \oplus Y \oplus Bin$

Borrow :-



$\Rightarrow \bar{X}Y + \bar{X}B + YB$

$\Rightarrow \bar{A}B + \bar{A}C + BC$

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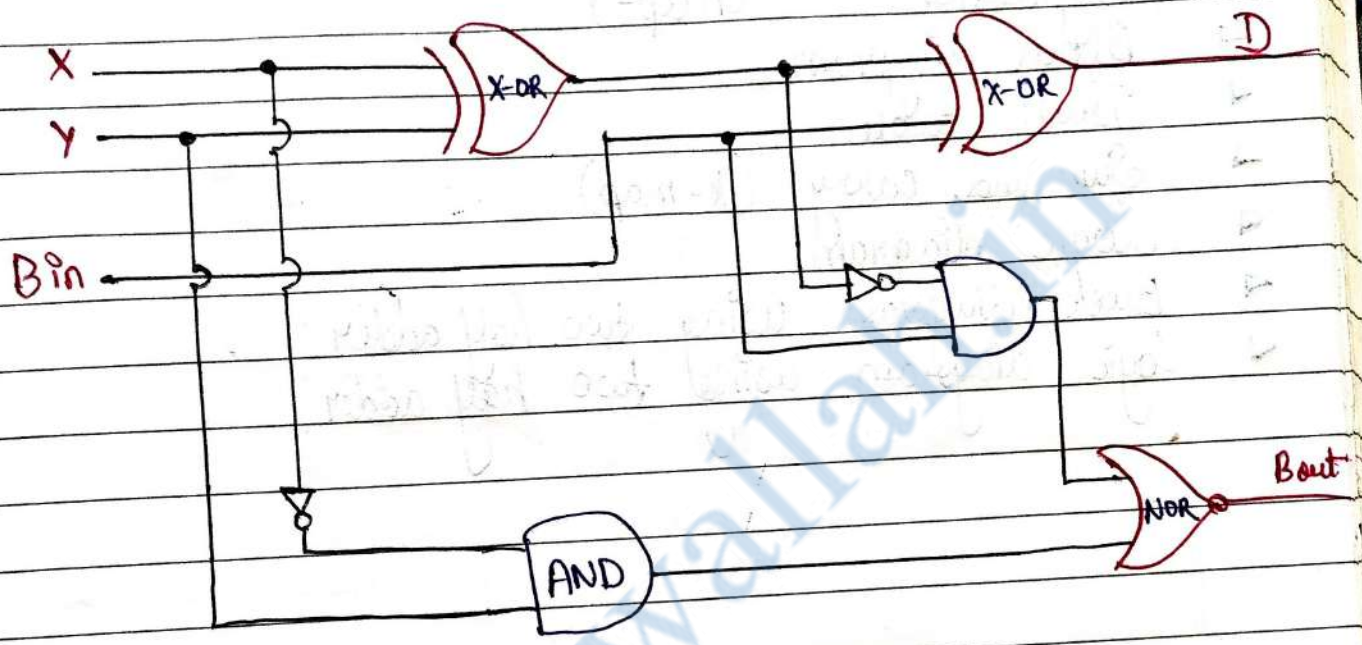
Two half subtracter = Full subtracter



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Steps of half and full adder/ Subtractor.....

- Defination (concept)
- Block diagram
- Truth table
- Sum and carry (k-map)
- logic diagram
- Block diagram using two half adder
- Logic diagram using two half adder

01/09/24

Unit - 3

Arithmetic Circuits

1) Explain half adders with truth table and logic gates. Realize half adder using (a) only NAND gates and (b) only NOR gates. (2015)

Sol'n => The half-adder: A half adder is a combinational circuit with two binary inputs (augend and added bits) and two binary outputs (sum and carry bits). It adds the two inputs (A and B) and produces the sum (S) and the carry (C) bits.

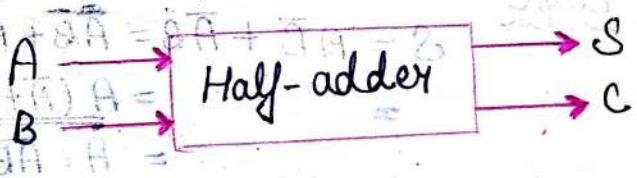
It is an arithmetic circuit used to perform the arithmetic operation of addition of two single bit words. The truth table and block diagram of a half-adder are shown below:-

Truth Table

Inputs		Output	
A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Half Adder

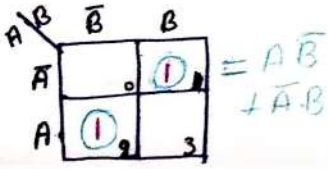
Block diagram



The sum (S) bit and the carry (C) bit, according to the rules of binary addition, are given by the sum (S) is the X-OR of A and B (It represents the LSB of the sum).

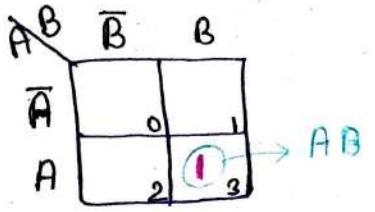
Therefore,

$$S = A\bar{B} + \bar{A}B = A \oplus B$$

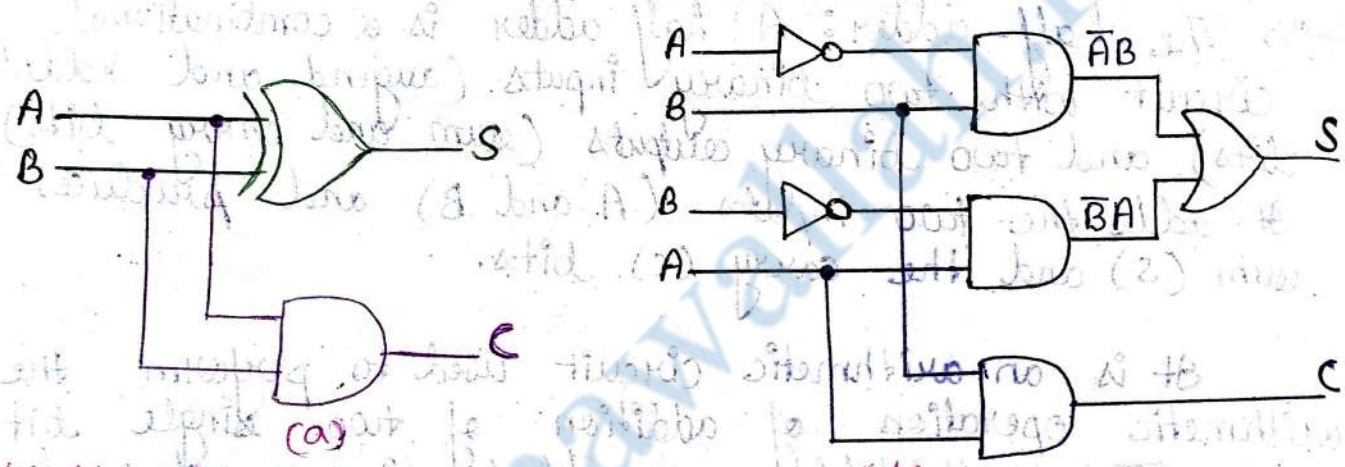


The carry (C) is the AND of A and B (It is 0 unless both the inputs are 1). Therefore,

$$C = AB$$



A half adder can, therefore, be realized by using one X-OR gate and one AND gate as shown below (a)....
Realization using AOI logic is shown below (b)....



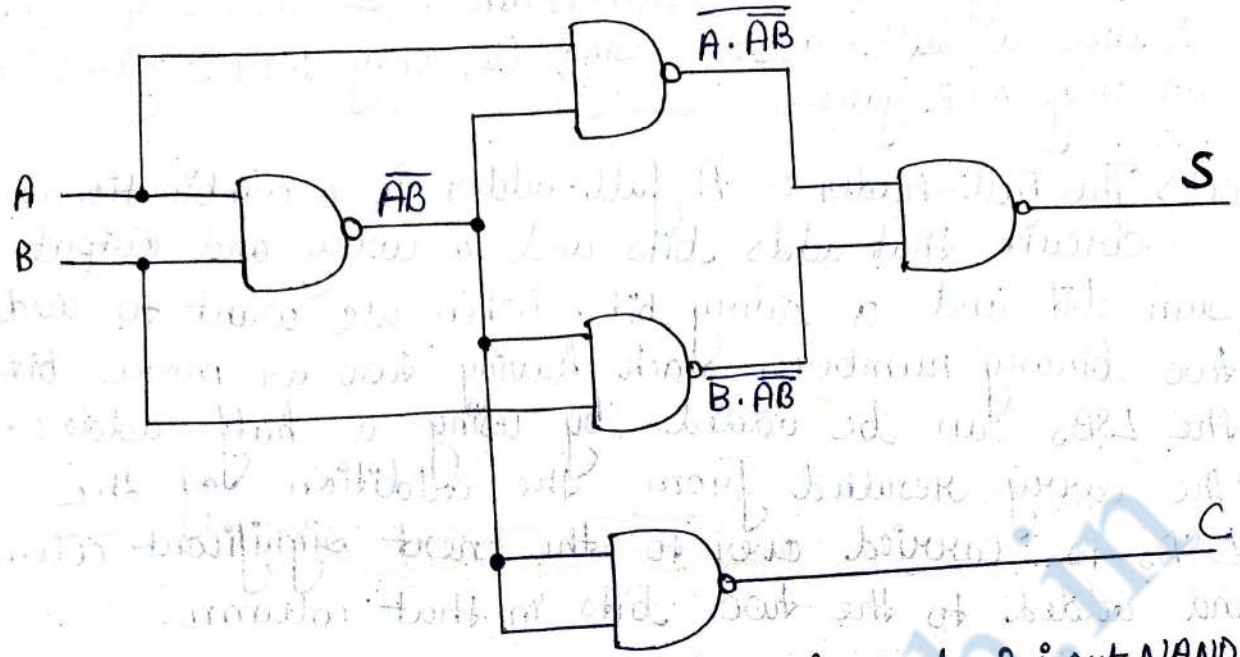
Half Adder

A half-adder can also be realized in universal logic by using either only NAND gates or only NOR gates as shown in figure 3 and 4 respectively.

NAND Logic

$$S = A\bar{B} + \bar{A}B = A\bar{A} + A\bar{B} + \bar{A}B + B\bar{B}$$
$$= A(\bar{A}+\bar{B}) + B(\bar{A}+\bar{B})$$
$$= \overline{\bar{A}\cdot\overline{A\bar{B}} + B\cdot\overline{A\bar{B}}} \quad (\bar{\bar{A}} = A)$$
$$= \overline{\overline{A\cdot\overline{A\bar{B}}}\cdot\overline{B\cdot\overline{A\bar{B}}}}$$

$$C = AB = \overline{\overline{AB}}$$



③ Logic diagram of a half-adder using only 2-input NAND gate

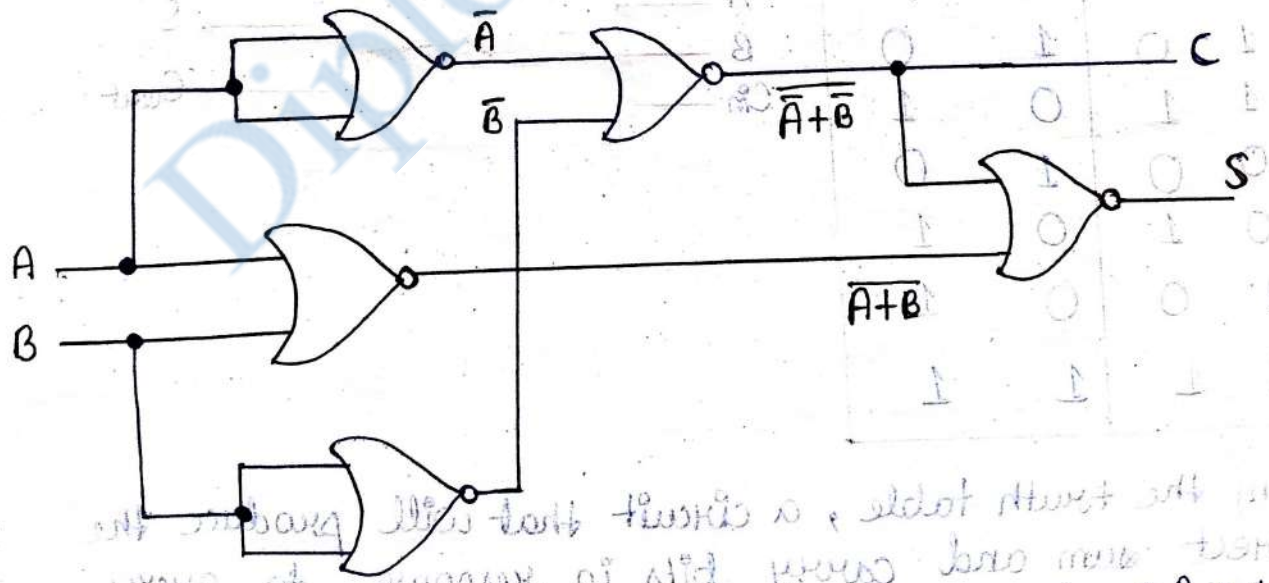
NOR Logic $S = A\overline{B} + \overline{A}B = \overline{A}B + A\overline{A} + \overline{A}B + B\overline{B}$

$= A(\overline{A}+\overline{B}) + B(\overline{A}+\overline{B})$

$= (A+B)(\overline{A}+\overline{B})$

$= \overline{\overline{A+B} + \overline{\overline{A}+\overline{B}}}$

$C = AB = \overline{\overline{AB}} = \overline{\overline{A}+\overline{B}}$



④ Logic diagram of a half-adder using only 2-input NOR gates.....

2) Explain full adders with truth table and logic gates. Realize a full-adders using (a) only NAND gates and (b) only NOR gates..... (2019)

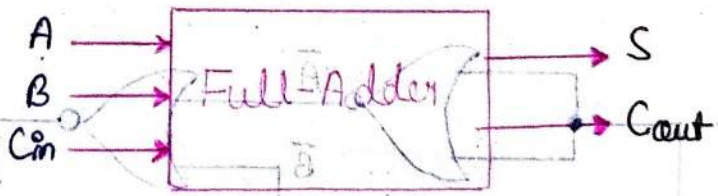
Soln ⇒ The Full-Adder :- A full-adder is a combinational circuit that adds bits and a carry and output a sum bit and a carry bit. When we want to add two binary numbers, each having two or more bits, the LSBs can be added by using a half-adder. The carry resulted from the addition of the LSBs is carried over to the next significant column and added to the two bits in that column.

So, in the second and higher columns, the two data bits of that column and the carry bit generated from the addition in the previous column need to be added.

Truth table

Inputs			Sum	Carry
A	B	Cin	S	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Full Adder Block diagram



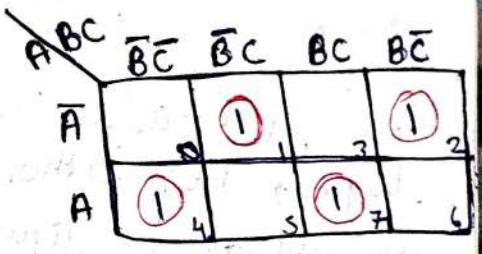
From the truth table, a circuit that will produce the correct sum and carry bits in response to every possible combination of A, B, and Cin is

$$S = \overline{ABC}in + \overline{A}B\overline{C}in + A\overline{B}Cin + ABCin$$

$$** = (A\overline{B} + \overline{A}B)\,\overline{C}in + (AB + \overline{AB})\,Cin$$

$$= (A \oplus B)\,\overline{C}in + (\overline{A \oplus B})\,Cin$$

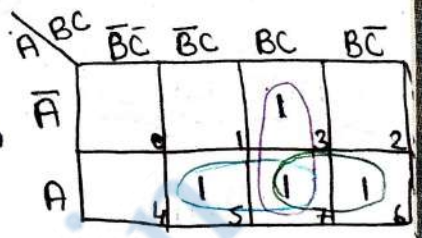
$$= A \oplus B \oplus Cin$$



and

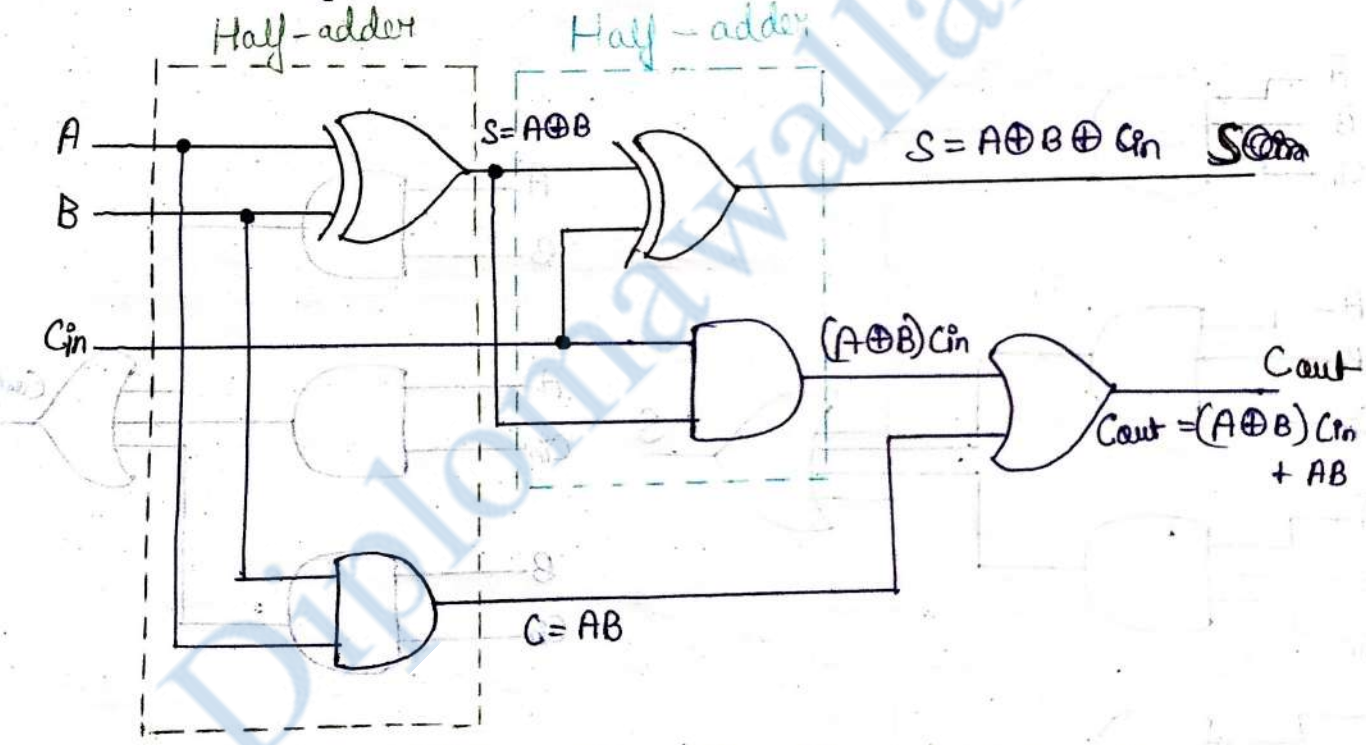
$$Cout = \bar{A}BCin + A\overline{B}Cin + AB\overline{C}in + ABCin$$

$$= AB + (A \oplus B)\,Cin = AB + + ACin + BCin$$



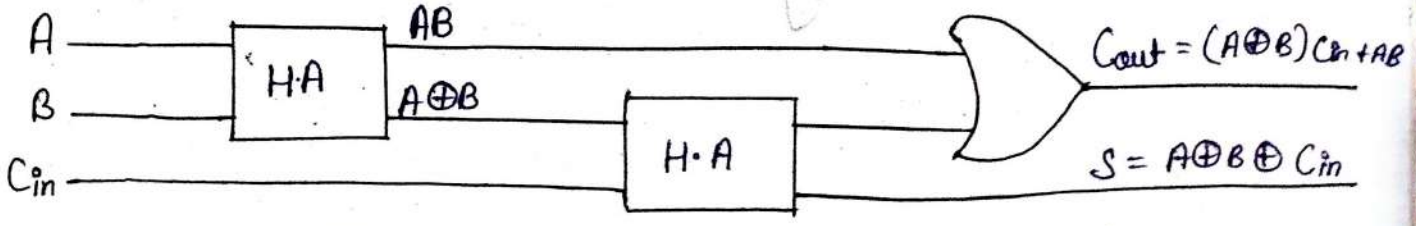
Logic diagram of full adder in college copy :-----

The logic diagram of the full-adder using two X-OR gates and two AND gates (i.e. two half adders) and one OR gate is shown in figure 2... below.....



② Logic diagram of a full-adder using two half-adder....

The block diagram of a full-adder using two half-adders is shown in figure ③.....



③ Block diagram of full-adder using two half-adder....

~~The full-adder can be constructed using two half-adders as~~

The full-adder can also be realized using universal logic, i.e, either only NAND gates or only NOR gates as shown in figure 5 and 6 respectively.

NAND Logic: $A \oplus B = \overline{\overline{A \cdot \overline{AB}} \cdot \overline{B \cdot \overline{AB}}}$

then,

$$S = A \oplus B \oplus C_{in} = \overline{\overline{(A \oplus B) \cdot \overline{(A \oplus B) C_{in}}} \cdot \overline{C_{in} (A \oplus B) C_{in}}}$$

$$C_{out} = C_{in} (A \oplus B) + AB = \overline{\overline{C_{in} \; A \oplus B} \cdot \overline{AB}}$$

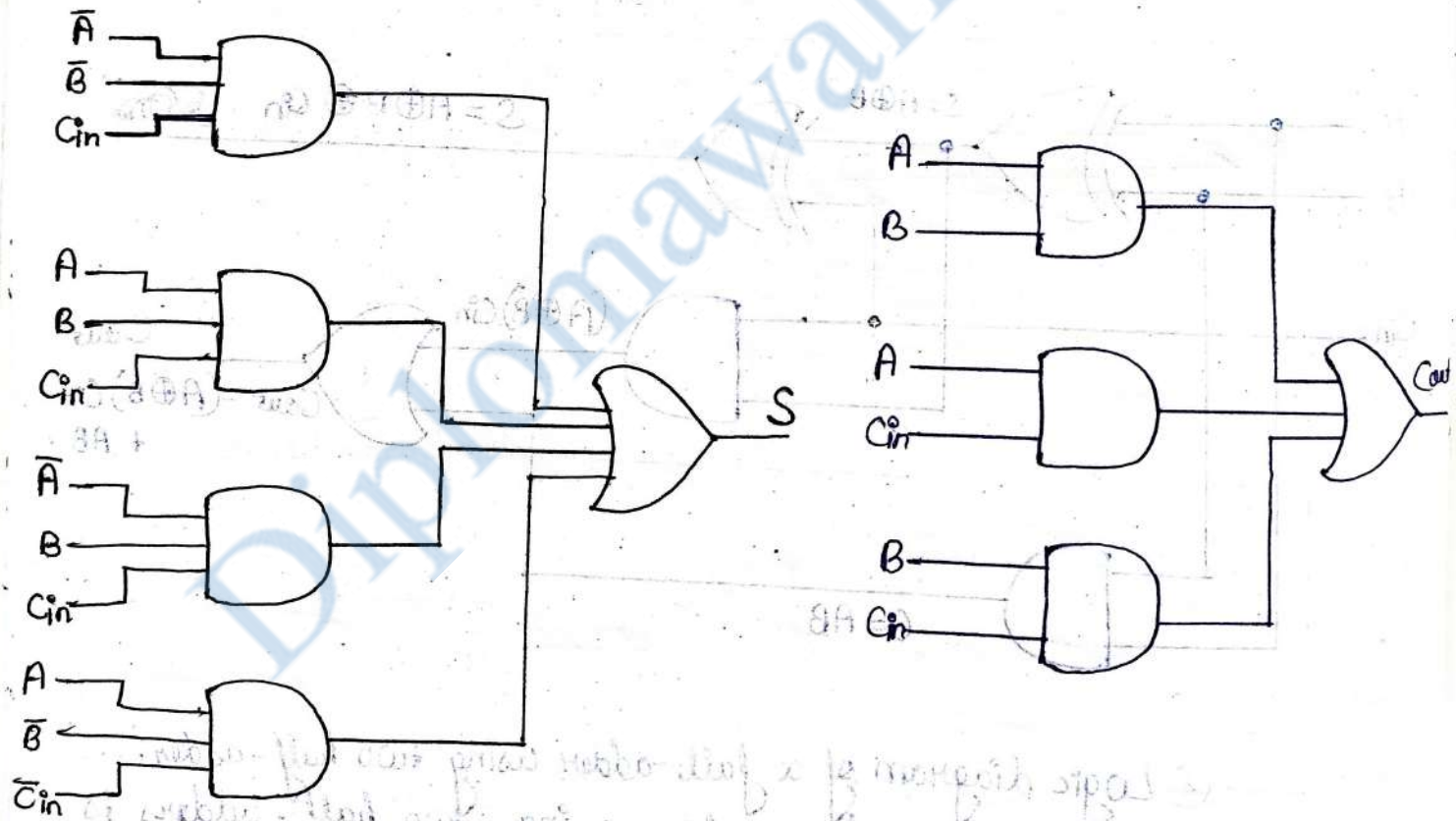


Figure: 4:- Sum and carry bits of a full-adder using AOI logic

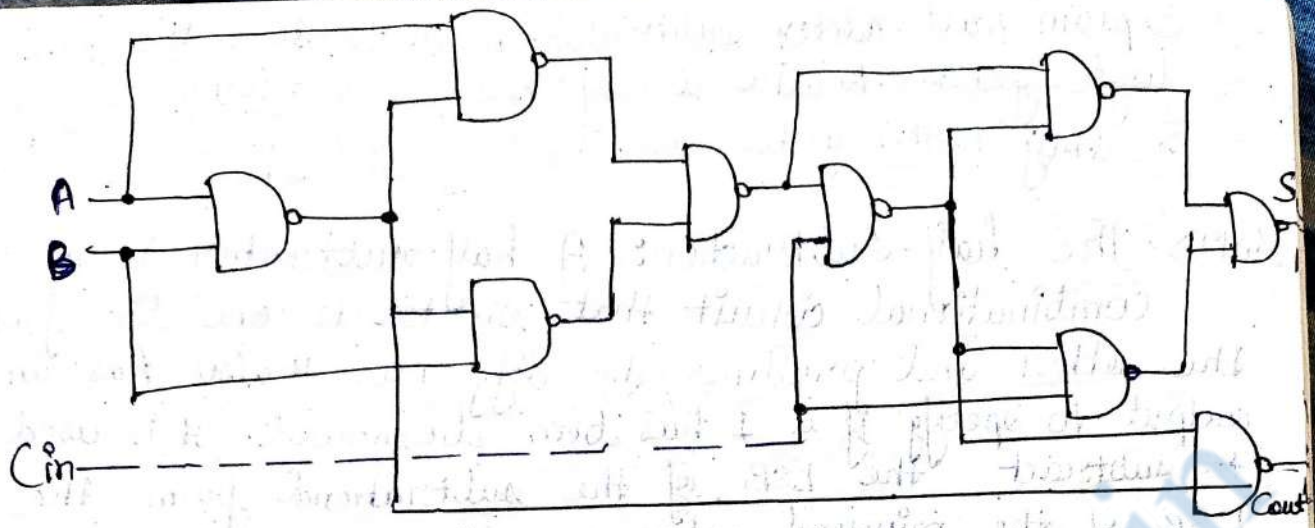


Figure:5:- Logic diagram of a full-adder using 2-input NAND gates:-

NOR logic : $A \oplus B = \overline{(\overline{A+B}) + \overline{\overline{A}+\overline{B}}}$

Then,

$S = A \oplus B \oplus C_{in} = \overline{(\overline{A \oplus B}) + C_{in}} + \overline{(\overline{A \oplus B}) + \overline{C}_{in}}$

$C_{out} = AB + C_{in}(A \oplus B) = \overline{\overline{A}+\overline{B}} + \overline{\overline{C}_{in} + \overline{A \oplus B}}$

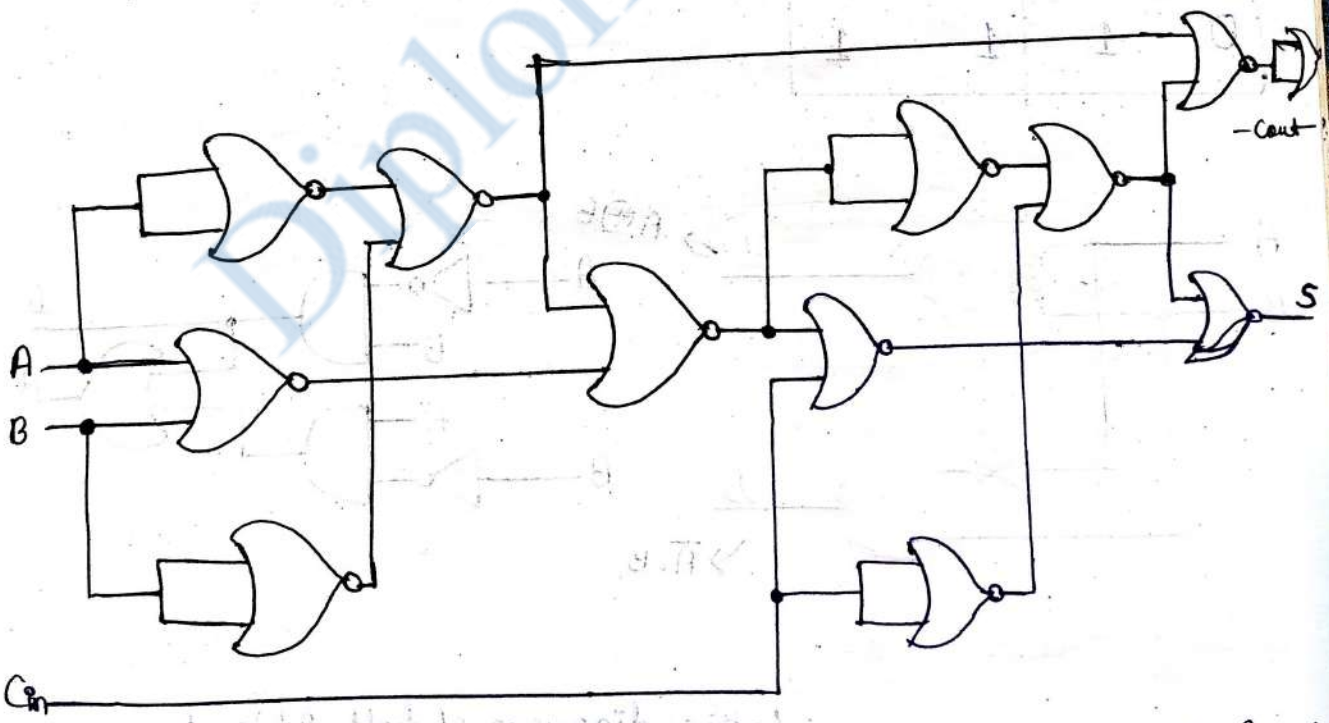


Figure:6: Logic diagram of a full-adder using only 2-input NOR gates....

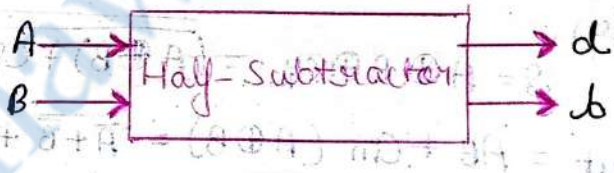
3.) Explain half-adder subtractor with truth table and logic gates. Realize a half-adder subtractor using (a) only NAND gates and (b) only NOR gates. . . (2018)

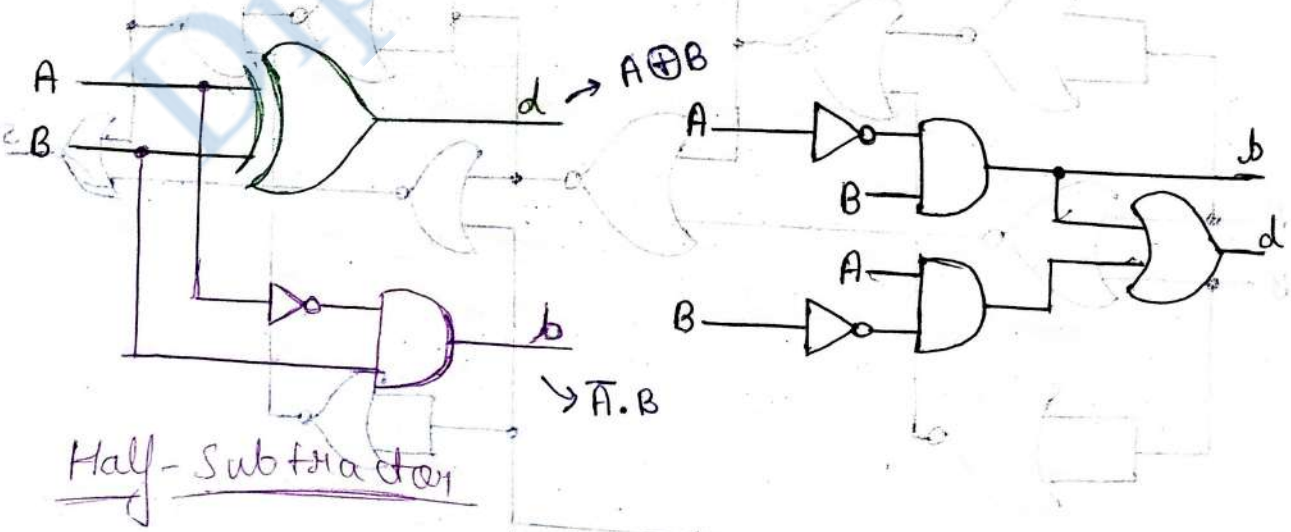
Soln ⇒ The half-Subtractor: A half-subtractor is a combinational circuit that subtracts one bit from the other and produces the difference. It also has an output to specify if a 1 has been borrowed. It is used to subtract the LSB of the subtrahend from the LSB of the minuend when one binary number is subtracted from the other. . .

Truth table

Inputs		Outputs	
A	B	d	b
0	0	0	0
1	0	1	0
1	1	0	0
0	1	1	1

Half subtractor
Block diagram





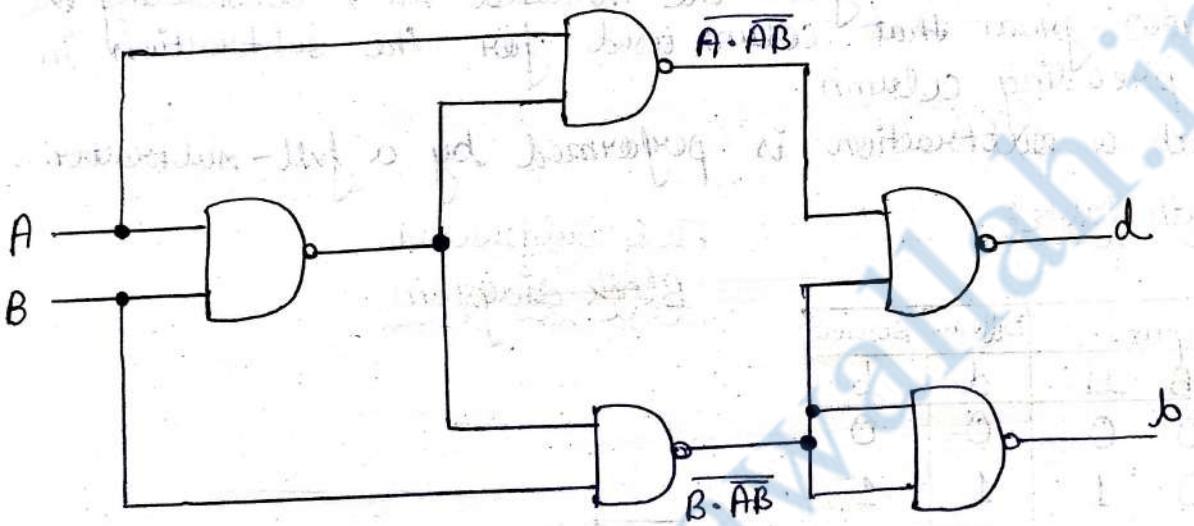
Half-Subtractor

Logic diagram of half-subtractor

A half subtractor can also be realized using universal logic - either using only NAND gates or using only NOR gates - as shown in figure 3 & 4 respectively.....

NAND logic : $d = A \oplus B = \overline{\overline{A \cdot \overline{AB}} \cdot \overline{B \cdot \overline{AB}}}$

$b = \overline{A}B = B(\overline{A} + \overline{B}) = B(\overline{AB}) = \overline{B \cdot \overline{AB}}$

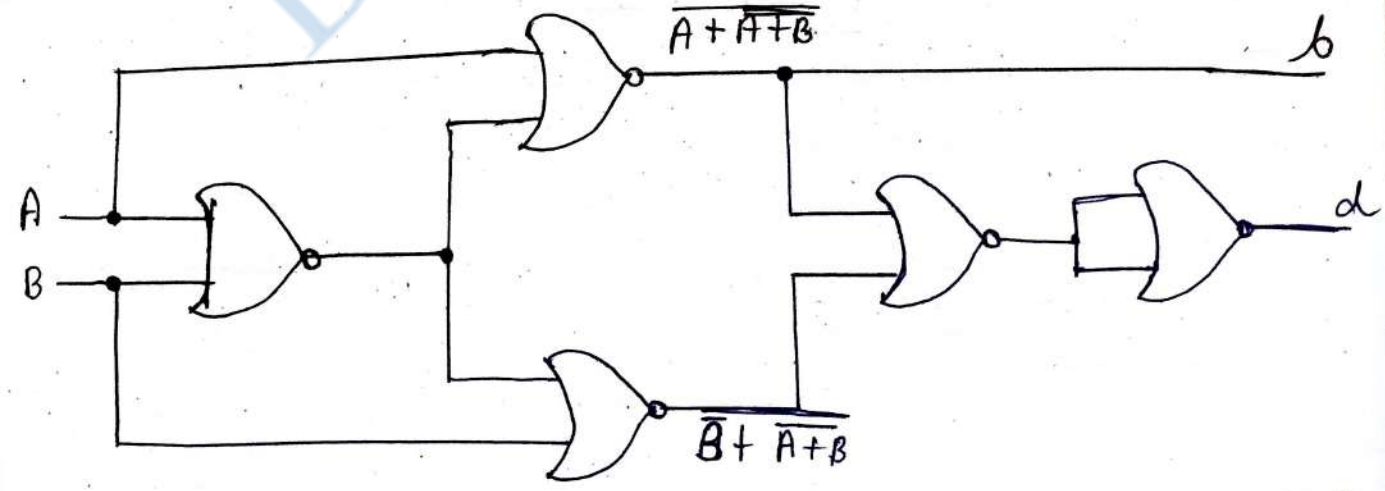


Logic diagram of half subtractor using only 2-input NAND gates.....

NOR logic : $d = A \oplus B = A\overline{B} + \overline{A}B = A\overline{B} + B\overline{B} + \overline{A}B + A\overline{A}$

$= \overline{B}(A+B) + \overline{A}(A+B) = \overline{B + \overline{A+B}} + \overline{A + \overline{A+B}}$

$d = \overline{A}B = \overline{A}(A+B) = \overline{\overline{A}(A+B)} = \overline{A + (\overline{A+B})}$



Logic diagram of a half-subtractor using only 2-input NOR gates.

4) Explain Full-subtractor with truth table and logic gates. Realize a full-subtractor using (a) only NAND gates and (b) only NOR gates..... (2017)

Sol⁽ⁿ⁾⇒ The full-Subtractor: The full-subtractor can be used only for LSB subtraction. If there is a borrow during the subtraction of the LSBs, it affects the subtraction in next higher column, the subtrahend bit is subtracted from the minuend bit, considering the borrow from that colum used for the subtraction in the preceding column.

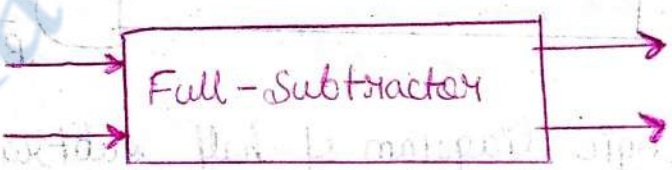
Such a subtraction is performed by a full-subtractor...

Truth table:

Inputs			Difference	Borrow
A	B	b_i	d	b
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

Full Subtractor

Block diagram



5.) Difference between a half adder and full-adder.

Parameter	Half adder	Full Adder
Definition	A combinational logic circuit that computes the addition of two binary digits is called as a Half-Adder.	A combinational logic circuit that computes the addition of three binary digits is called as a Full-adder.
Inputs	A half adder has two inputs (A and B).	A Full adder has three inputs A, B and Cin.
Outputs	A half adder has two outputs S (Sum) and C (Carry).	A Full adder has two outputs S (sum) and Cout (carry).
Carry input	Half adder does not have carry input.	Full adder has carry input.
Components used	Half adder uses one EX-OR and one AND gate for its implementation	Full adder uses two EX-OR gates, two AND gates and one OR gate for its implementation.
Boolean Expression	S (Sum) = $A \oplus B = A\bar{B} + \bar{A}B$ C (carry) = AB.	S (Sum) = $A \oplus B \oplus C_{in}$ C (Carry) = $AB + AC_{in} + BC_{in}$
Logic gates used	The number of logic gates used is less.	The number of logic gates used is more.
Applications	1. Constructing full adders. 2. Computer ALU	1. Arithmetic Logic Unit 2. Digital Calculators 3. Digital Computers 4. Digital signal processors.

6.) With the help of a block diagram explain the work of a serial adder...